1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
E		408395	PRODUCTION RELEASED	11/02/05	?

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table Of Contents	N/A	N/A
2	2	Board Information	N/A	N/A
3	3	System Block Diagram	MARIAS	08/24/2005
4	4	Power Block Diagram	MARIAS	08/24/2005
5	5	Revision History	N/A	N/A
6	6	Q41C Pin Swaps	N/A	N/A
7	7	Functional Test Points	MARIAS	08/24/2005
8	8	I2C Connections	MARIAS	08/24/2005
9	9	JTAG Connections	MARIAS	08/24/2005
10	10	Power Synonyms	MARIAS	08/24/2005
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12	12	Power Inputs	MARIAS	08/24/2005
13	13	Battery Charger	MARIAS	08/24/2005
14	14	12.8V PBUS/PMU Supplies	MARIAS	08/24/2005
15	15	5V/3.3V Supplies	MARIAS	08/24/2005
16	16	1.8V/1.5V Supplies	MARIAS	08/24/2005
17	17	2.5V Supply	MARIAS	08/24/2005
18	19	Vesta Power & Misc	MARIAS	08/24/2005
19	21	I2 Power	MARIAS	08/24/2005
20	22	I2 Power Supplies	MARIAS	08/24/2005
21	23	I2 Supplemental	MARIAS	08/24/2005
22	24	I2 Miscellaneous	MARIAS	08/24/2005
23	25	PCI Clock Buffer	MARIAS	08/24/2005
24	26	LEDs/Reset/Debug	MARIAS	08/24/2005
25	27	Power Management Unit (PMU05)	MARIAS	08/24/2005
26	29	Power Sequencing	MARIAS	08/24/2005
27	30	Fan Controller	MARIAS	08/24/2005
28	31	ALS Support	MARIAS	08/24/2005
29	32	Sudden Motion Sensor	MARIAS	08/24/2005
30	33	Q41C Internal I/O I	N/A	N/A
31	34	Q41C Internal I/O II	N/A	N/A
32	35	I2 Processor Interface	MARIAS	08/24/2005
33	36	A8 MaxBus (CPU0)	MARIAS	08/24/2005
34	37	A8 Configuration Straps	MARIAS	08/24/2005
35	38	A8 Power (CPU0)	MARIAS	08/24/2005
36	39	CPU VCore Supply	MARIAS	08/24/2005
37	46	CPU AVDD Supply	MARIAS	08/24/2005
38	47	I2 Memory Interface	MARIAS	08/24/2005
39	48	Memory Series Termination	MARIAS-NDIFF	N/A
40	50	DDR2 SO-DIMM Slot A	MARIAS-MDIFF	N/A
41	52	DDR2 SO-DIMM Slot B	MARIAS-MDIFF	N/A
42	55	M11 Frame Buffer Constraints	MARIAS	08/24/2005
43	56	I2 AGP Interface	MARIAS	08/24/2005
44	57	GPU (M11) AGP Interface	MARIAS	08/24/2005
45	58	GPU VCore Supply	MARIAS	08/24/2005
46	59	GPU (M11) Core Power	MARIAS	08/24/2005
47	60	GPU (M11) I/O Power	MARIAS	08/24/2005
48	61	GPU (M11) Frame Buffer I/F	MARIAS	08/24/2005
49	62	GPU Frame Buffer A	MARIAS	08/24/2005
50	63	GPU Frame Buffer B	MARIAS	08/24/2005
51	64	GPU (M11) GPIOs/Straps	MARIAS	08/24/2005
52	65	GPU (M11) Clocks/Misc	MARIAS	08/24/2005
53	66	GPU (M11) DVI/DAC Outputs	MARIAS	08/24/2005
54	67	Lower TMDS Transmitter	MARIAS	08/24/2005
55	68	Upper TMDS Transmitter	MARIAS	08/24/2005
56	69	Internal Display Conns	MARIAS	08/24/2005
57	70	External Display Conns	MARIAS-PDIFF	06/02/2005
58	71	BootROM	MARIAS	08/24/2005
59	72	I2 PCI Interface	MARIAS	08/24/2005
60	73	Q85 AIRPORT/BT CONN	MARIAS-MDIFF	N/A
61	74	Cardbus	MARIAS	08/24/2005
62	75	NEC USB2	MARIAS	08/24/2005
63	81	I2 UATA Interface	MARIAS	08/24/2005
64	82	HDD/ODD Connectors	MARIAS-PDIFF	06/02/2005
65	84	I2 Ethernet Interface	MARIAS	08/24/2005
66	85	Vesta Ethernet PHY	MARIAS	08/24/2005
67	86	Ethernet Connector	N/A	N/A
68	88	I2 FireWire Interface	MARIAS	08/24/2005
69	89	Vesta FireWire PHY	MARIAS	08/24/2005
70	90	FireWire Ports	MARIAS-PDIFF	06/02/2005
71	91	FireWire Series Term	MARIAS	08/24/2005
72	92	I2 USB Interface	MARIAS	08/24/2005
73	93	NEC USB2 Interface	MARIAS	08/24/2005
74	100	Audio Board Connector	N/A	N/A
75	110	Spacing & Physical Constraints	MARIAS	08/24/2005
76	111	Spacing & Physical Constraints 2	MARIAS	08/24/2005
77	112	Cross Reference Page		
78	113	Cross Reference Page		
79	114	Cross Reference Page		
80	115	Cross Reference Page		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6839	1	SCHEM,BOZEMAN,Q41C	SCH1		
820-1810	1	PCBF,BOZEMAN,Q41C	PCB1	CRITICAL	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:SYV]	CRITICAL	EEE_SYV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:TML]	CRITICAL	EEE_TML
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USH]	CRITICAL	EEE_USH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USJ]	CRITICAL	EEE_USJ

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE
SCHEM,MLB,PB17"

DRAWING NUMBER 051-6839 REV. E

Design-Specific Rules

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
    STANDARD    =DEFAULT    *    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT
TABLE_SPACING_RULE
    BGA_P1MM    10    *    0.10 MM    1.25 MM    0.1 MM    12.5 MM    15.0 MM
TABLE_SPACING_RULE
    BGA_P2MM    20    *    0.20 MM    1.25 MM    0.1 MM    12.5 MM    15.0 MM
TABLE_SPACING_RULE
    DEFAULT    *    0.1 MM    2.5 MM    0.15 MM    10.0 MM    15.0 MM
TABLE_SPACING_ASSIGNMENT

TABLE_SPACING_ASSIGNMENT
    *    *    1MM    BGA_P1MM
TABLE_SPACING_ASSIGNMENT
    AGP_STB    *    1MM    BGA_P2MM
TABLE_SPACING_ASSIGNMENT
    CLOCK    *    1MM    BGA_P2MM
TABLE_SPACING_ASSIGNMENT
    RAM_DIFF    *    1MM    BGA_P2MM
```

"1MM" area defined around BGAs to reduce DRCs caused by fan-out.

"BGA_P2MM" rule ensures these critical signals do not fan-out routed next to any other signals.

```
TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    STANDARD    *    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT
TABLE_PHYSICAL_RULE
    DEFAULT    *    Y    0.100 MM    0.100 mm    1.25 MM
```

Layer-specific rules for 90-ohm differential impedance

```
TABLE_SPACING_RULE

TABLE_SPACING_RULE
    90_OHM_DIFF    TOP,BOTTOM    2.5 MM    0.200 MM    2.5 MM    1.0 MM
TABLE_SPACING_RULE
    90_OHM_DIFF    *    2.5 MM    0.200 MM    2.5 MM    1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    90_OHM_DIFF    TOP,BOTTOM    Y    0.118 MM    0.1 MM    5 MM
TABLE_PHYSICAL_RULE
    90_OHM_DIFF    *    Y    0.125 MM    0.1 MM    5 MM
```

Layer-specific rules for 100-ohm differential impedance

```
TABLE_SPACING_RULE

TABLE_SPACING_RULE
    100_OHM_DIFF    TOP,BOTTOM    2.5 MM    0.200 MM    2.5 MM    1.0 MM
TABLE_SPACING_RULE
    100_OHM_DIFF    *    2.5 MM    0.200 MM    2.5 MM    1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    100_OHM_DIFF    TOP,BOTTOM    Y    0.092 MM    0.1 MM    5 MM
TABLE_PHYSICAL_RULE
    100_OHM_DIFF    *    Y    0.100 MM    0.1 MM    5 MM
```

Layer-specific rules for 110-ohm differential impedance

```
TABLE_SPACING_RULE

TABLE_SPACING_RULE
    110_OHM_DIFF    TOP,BOTTOM    2.5 MM    0.330 MM    2.5 MM    1.0 MM
TABLE_SPACING_RULE
    110_OHM_DIFF    *    2.5 MM    0.300 MM    2.5 MM    1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    110_OHM_DIFF    TOP,BOTTOM    Y    0.080 MM    0.1 MM    5 MM
TABLE_PHYSICAL_RULE
    110_OHM_DIFF    *    Y    0.085 MM    0.1 MM    5 MM
```

Portable-specific Override Rules

```
TABLE_SPACING_RULE

TABLE_SPACING_RULE
    AGP    201    *    0.2 MM
TABLE_SPACING_RULE
    AGP_STB    251    *    0.25 MM
TABLE_SPACING_RULE
    VGA    151    *    0.15 MM    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT
TABLE_SPACING_RULE
    TV    151    *    0.15 MM    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    VGA    *    =60_OHM_SE    =60_OHM_SE    =60_OHM_SE    =60_OHM_SE
TABLE_PHYSICAL_RULE
    TV    *    =60_OHM_SE    =60_OHM_SE    =60_OHM_SE    =60_OHM_SE
```

Layer-specific rules for 60-ohm single-ended impedance

```
TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    60_OHM_SE    *    Y    0.076 MM    =50_OHM_SE    =50_OHM_SE
```

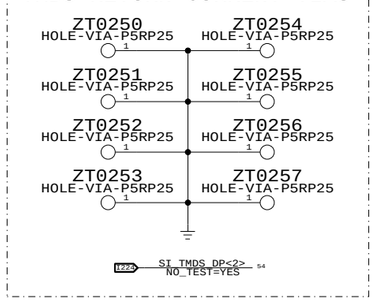
Layer-specific rules for 50-ohm single-ended impedance

```
TABLE_SPACING_RULE

TABLE_SPACING_RULE
    50_OHM_SE    *    2.5 MM    0.125 MM    2.5 MM    1.0 MM
TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    50_OHM_SE    *    Y    0.100 MM    0.100 MM    1.25 MM
```

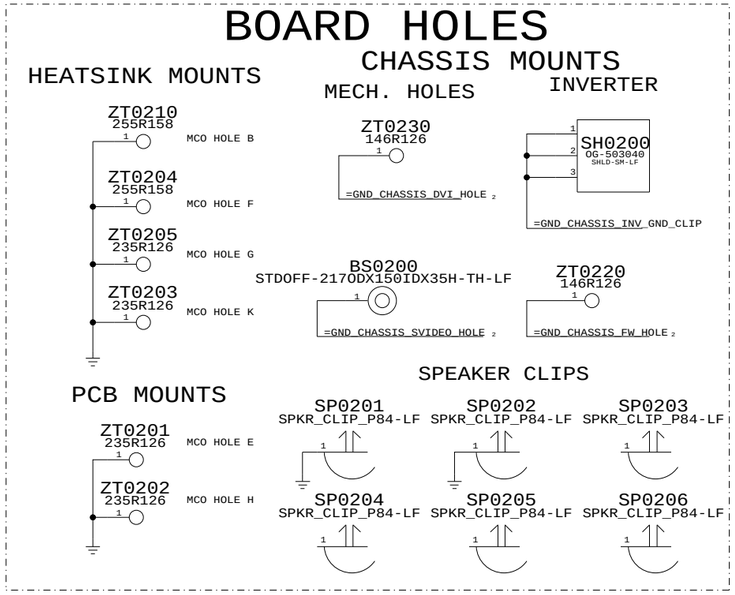
CHASSIS GND CONNECTIONS

```
GND_CHASSIS_UPPER_DVI
    MAKE_BASE=TRUE
    VOLTAGE=0V
    MIN_LINE_WIDTH=0.6 mm
    MIN_NECK_WIDTH=0.25 mm
    =GND_CHASSIS_DVI_HOLE 2
    =GND_CHASSIS_DVI2 57
    =GND_CHASSIS_DVI3 57

GND_CHASSIS_FW_LOWER_DVI
    MAKE_BASE=TRUE
    VOLTAGE=0V
    MIN_LINE_WIDTH=0.6 mm
    MIN_NECK_WIDTH=0.25 mm
    =GND_CHASSIS_FW_HOLE 2
    =GND_CHASSIS_DVI1 57
    =GND_CHASSIS_DVI4 57
    =GND_CHASSIS_TV 57
    =GND_CHASSIS_ENET 67
    =GND_CHASSIS_FW_PORT1 70
    =GND_CHASSIS_FW_PORT2 70
    =GND_CHASSIS_FW_EMI 70
    =GND_CHASSIS_SVIDEO_HOLE 2

GND_CHASSIS_LCD
    MAKE_BASE=TRUE
    VOLTAGE=0V
    MIN_LINE_WIDTH=0.6 mm
    MIN_NECK_WIDTH=0.25 mm
    =GND_CHASSIS_LCD1 56
    =GND_CHASSIS_LCD2 56
    =GND_CHASSIS_LCD3 56
    =GND_CHASSIS_LCD4 56

GND_CHASSIS_INVERTER
    MAKE_BASE=TRUE
    VOLTAGE=0V
    MIN_LINE_WIDTH=0.6 mm
    MIN_NECK_WIDTH=0.25 mm
    =GND_CHASSIS_INV_GND_CLIP 2
    =GND_CHASSIS_INVERTER1 56
    =GND_CHASSIS_INVERTER2 56
```

TMDS RETURN CURRENT VIAS



BOARD HOLES



BOARD STACK-UP AND CONSTRUCTION

SEE BOARD FILE FOR DETAILED INFORMATION
CONVENTIONAL CONSTRUCTION WITH Pxx TH VIA

1		SIGNAL (1/2 OZ + COPPER PLATING)
2	PREPREG	GROUND (1/2 OZ)
3	CORE	SIGNAL (1/2 OZ)
4	PREPREG	SIGNAL (1/2 OZ)
5	CORE	GROUND (1/2 OZ)
6	PREPREG	CUT POWER PLANE (1 OZ)
7	CORE	CUT POWER PLANE (1 OZ)
8	PREPREG	GROUND (1/2 OZ)
9	CORE	SIGNAL (1/2 OZ)
10	PREPREG	SIGNAL (1/2 OZ)
11	CORE	GROUND (1/2 OZ)
12	PREPREG	SIGNAL (1/2 OZ + COPPER PLATING)

```
TABLE_BOARD_INFO
    TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM    NO_TYPE,1MM    MM
```

BOM OPTIONS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7017	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_S,Q41C	COMMON,ALTERNATE,EEE_SYV,GPU_LF,VRAM_SAMSUNG,gQ41C,gCommon
630-7186	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_H,Q41C	COMMON,ALTERNATE,EEE_TML,GPU_LF,VRAM_HYNIX,gQ41C,gCommon
630-7443	PCBA,MLB,BESTMHZ,GPU_EUT,VRAM_S,PB17	COMMON,ALTERNATE,EEE_USH,GPU_EUTECTIC,VRAM_SAMSUNG,gQ41C,gCommon
630-7444	PCBA,MLB,BESTMHZ,GPU_EUT,VRAM_H,PB17	COMMON,ALTERNATE,EEE_USJ,GPU_EUTECTIC,VRAM_HYNIX,gQ41C,gCommon

BOM GROUP	BOM OPTIONS
gCommon	5V_HD_LOGIC,BACKUP_BATT,CPU_A7PM,I2_FW_BETA,I2_MAXBUS_50OHM,MAXBUS_1V8,gCommon1
gCommon1	MMM_ACCEL_KIONIX,GPU_PWRPLAY,GPU_SS,GPU_LVDDR_2V8,GPU_MEMIO_1V8,gCommon2
gCommon2	I2_REV1_NOT,I2_MAXBUS_FBCLK_MATCHED,I2_AGP_FBCLK_MATCHED,I2_PCI_FBCLK_MATCHED,gCommon3
gCommon3	CPU_VCORE_2STATES,I2_MAXBUS_166MHZ,CPU0_BUSRATIO_10.0X,I2VCORE_1V5,I2VCORE_BURST,gCommon4
gCommon4	VESTA_PORT2_DISABLE,DVO_1V8,TMDS_DUAL,VCORE_OFFSET,VCORE_OFFSET_SW,gUSB
gUSB	USB2_NEC,USB1P1_NEC,TPAD_SEQ_PMU
gQ41C	Q41C_PARTS,A7PM_1P67_LGA,BOOTROM_PROG,PMU_PROG,MAXBUS_TBEN_SYNC,gQ41CVcore
gQ41CVcore	CPU0_VCORE_1V30,Q41,CPU0_AVDD_1V30

Module Components

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0383	1	IC,ASIC,I2,REV1.2,NB/SB,974 BGA	U2100	CRITICAL	
337S3135	1	IC,PMU05,BLANK,QFP	U2700	CRITICAL	PMU_BLANK
341S1772	1	IC,PMU05,Vxxx,QFP	U2700	CRITICAL	PMU_PROG
337S3181	1	IC,A7PM,R1.5,1.67GHZ,LGA,1.28V,25W,85C	U3600	CRITICAL	A7PM_1P67_LGA
337S3077	1	IC,A8,xxxGHZ	U3600	CRITICAL	CPU_A8
338S0252	1	IC,GPU,M11P	U5700	CRITICAL	GPU_LF
338S0299	1	IC,GPU,M11P,EUTECTIC	U5700	CRITICAL	GPU_EUTECTIC
335S0088	1	BOOTROM,BLANK	U7100	CRITICAL	BOOTROM_BLANK
341S1739	1	IC,BOOTROM,B,Q41C	U7100	CRITICAL	BOOTROM_PROG
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U8500	CRITICAL	
333S0317	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_SAMSUNG
333S0314	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0388	343S0356	?	U8500	v1.4 is alt to v1.3

Board Information

SYNC_MASTER=N/A SYNC_DATE=N/A

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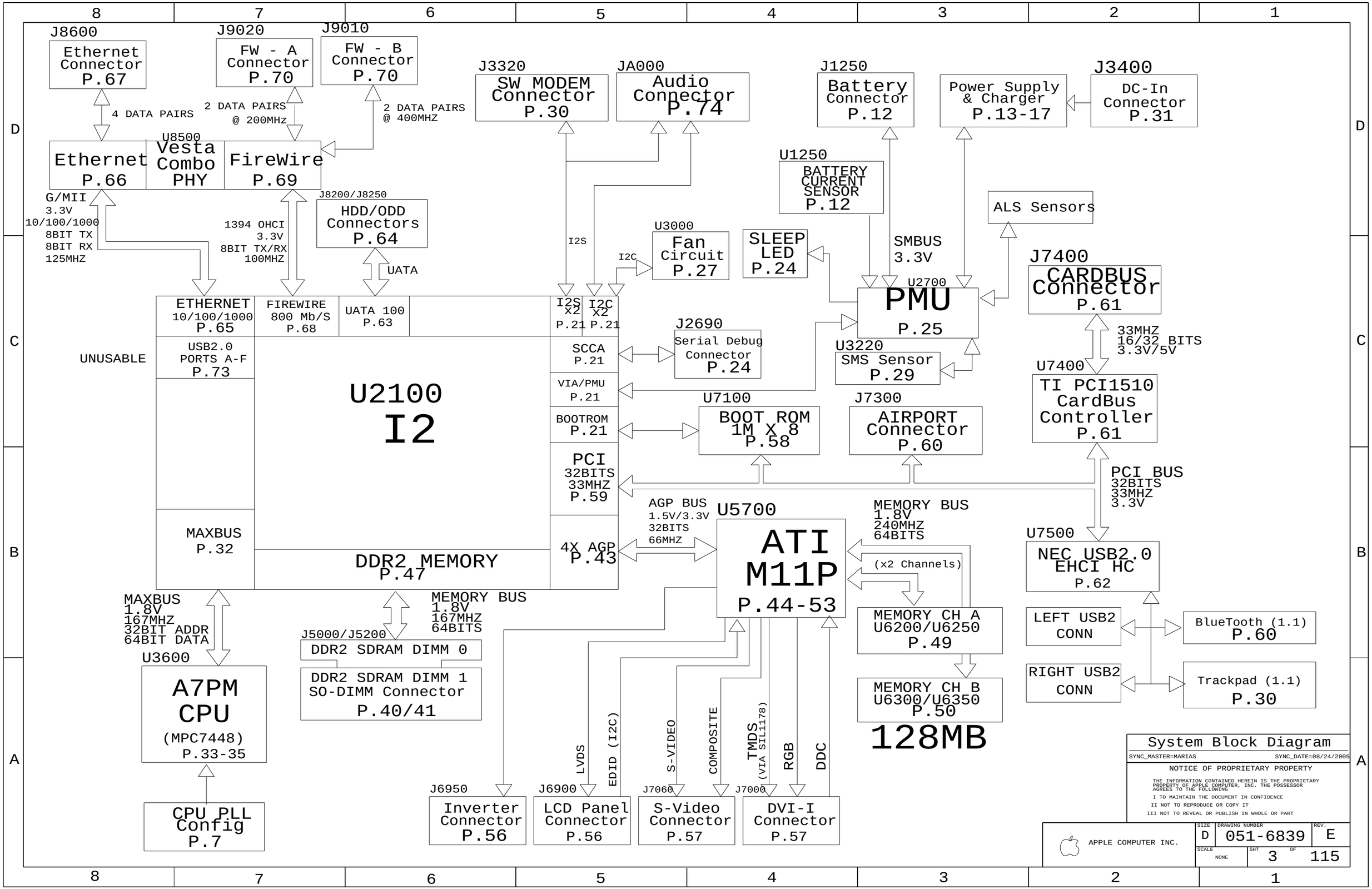
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 2 OF 115	


J8600
Ethernet Connector P.67
J9020
FW - A Connector P.70
J9010
FW - B Connector P.70
J3320
SW MODEM Connector P.30
JA000
Audio Connector P.74
J1250
Battery Connector P.12
Power Supply & Charger P.13-17
J3400
DC-In Connector P.31
4 DATA PAIRS
2 DATA PAIRS @ 200MHz
2 DATA PAIRS @ 400MHZ
U8500
Ethernet P.66
Vesta Combo PHY
FireWire P.69
U1250
BATTERY CURRENT SENSOR P.12
ALS Sensors
G/MII 3.3V 10/100/1000 8BIT TX 8BIT RX 125MHZ
1394 OHCI 3.3V 8BIT TX/RX 100MHZ
J8200/J8250
HDD/ODD Connectors P.64
UATA
I2S
I2C
U3000
Fan Circuit P.27
SLEEP LED P.24
SMBUS 3.3V
U2700
PMU P.25
J7400
CARDBUS Connector P.61
ETHERNET 10/100/1000 P.65
FIREWIRE 800 Mb/S P.68
UATA 100 P.63
I2S X2 P.21
I2C X2 P.21
J2690
Serial Debug Connector P.24
33MHZ 16/32 BITS 3.3V/5V
UNUSABLE
USB2.0 PORTS A-F P.73
SCCA P.21
U3220
SMS Sensor P.29
U7400
TI PCI1510 CardBus Controller P.61
U2100
I2
VIA/PMU P.21
U7100
BOOT ROM 1M X 8 P.58
J7300
AIRPORT Connector P.60
BOOTROM P.21
PCI 32BITS 33MHZ P.59
PCI BUS 32BITS 33MHZ 3.3V
AGP BUS 1.5V/3.3V 32BITS 66MHZ
U5700
MEMORY BUS 1.8V 240MHZ 64BITS
MAXBUS P.32
4X AGP P.43
DDR2 MEMORY P.47
ATI M11P P.44-53
(x2 Channels)
U7500
NEC USB2.0 EHCI HC P.62
MAXBUS 1.8V 167MHZ 32BIT ADDR 64BIT DATA
MEMORY BUS 1.8V 167MHZ 64BITS
J5000/J5200
DDR2 SDRAM DIMM 0
DDR2 SDRAM DIMM 1 SO-DIMM Connector P.40/41
MEMORY CH A U6200/U6250 P.49
MEMORY CH B U6300/U6350 P.50
128MB
LEFT USB2 CONN
BlueTooth (1.1) P.60
RIGHT USB2 CONN
Trackpad (1.1) P.30
U3600
A7PM CPU (MPC7448) P.33-35
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1178)
RGB
DDC
J6950
Inverter Connector P.56
J6900
LCD Panel Connector P.56
J7060
S-Video Connector P.57
J7000
DVI-I Connector P.57
CPU PLL Config P.7
System Block Diagram
SYNC_MASTER=MARIAS
SYNC_DATE=08/24/2005
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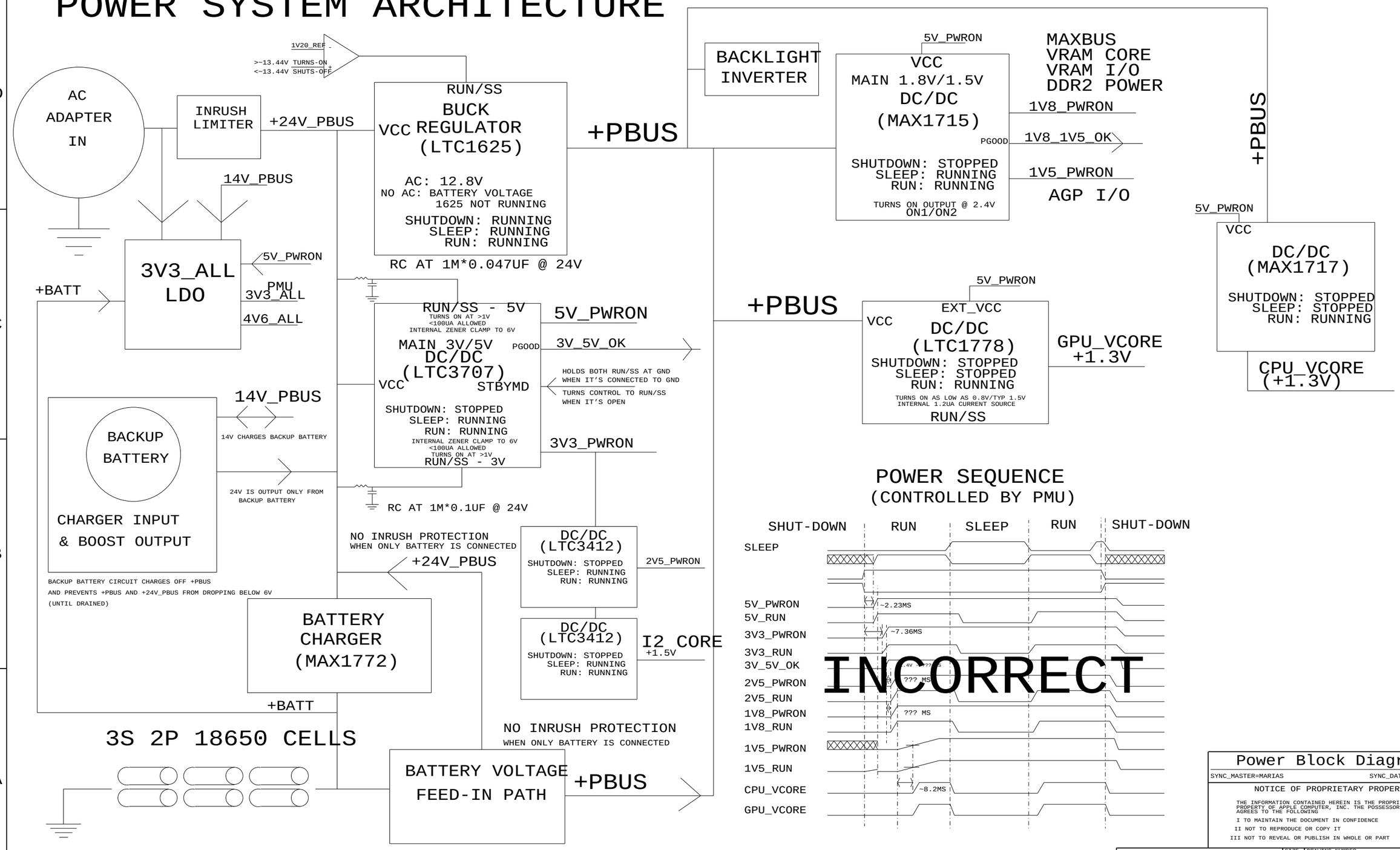
SIZE D
DRAWING NUMBER 051-6839
REV. E
SCALE NONE
SHT 3 OF 115

POWER SYSTEM ARCHITECTURE



Power Block Diagram

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 4 OF 115	

REVISION HISTORY

PROTO

```
04/05/2005 - Beginning revision history
           - Sync'd FB pin swaps from 051-5838
           - Pinned out audio connector per flex cable
           - Pinned out left USB/ALS connector per flex cable
04/07/2005 - Moved modem connector to non-shared page
           - Updated chassis ground connections
           - Pin swapped DDR2 according to layout
04/11/2005 - Changed audio caps to X5R (CA033, CA050, CA051)
04/12/2005 - Updated wireless connector pinout according to flex
           - Implemented more DDR2 pin swaps
           - Implemented pin swaps on FW data lines
           - Added RAM DQS_N pulldowns
           - Corrected mdsl line and neck width properties
04/14/2005 - Switched GPU to M11
04/15/2005 - Added CPU Vcore mux circuit
04/19/2005 - Added NO_TEST property to buses between JTAG enabled devices
           - Pinswapped FB V/P for M11
04/20/2005 - Corrected ENET power rail to PWRON instead of RUN (Wake-on-LAN)
           - Corrected Vesta reset and ethernet LOWPWR circuits
           - Changed Rs480 to 6.34k to take GPU Vcore to 1.3V/1.05V
           - Added page 6 and modified pages 11,35,51 for design specific pin swaps
           - Separated GPU MVREF into two dividers
04/26/2005 - Added 8 vias for TMDS return current
           - Added LVDS electrical constraint set properties
04/27/2005 - Added NO_TEST property to SI-TMDS-Rx (no room for TP)
           - Changed MIN_NECK_WIDTH property on TMDS power rails to 0.2 mm
           - Changed gender of debug connector
           - Removed C6367 due to MCO violation
04/29/2005 - Schematic released as REV 01 for PROTO
```

EVT

```
05/04/2005 - Added SYNONYMS to allow DVO and USB pulldown pinswaps
05/09/2005 - Added missing pullup to SYS_LID_OPEN
           - Added missing pulldown to Vesta LPWR 1394
05/09/2005 - Lead-free resistor replacement on page 86
05/16/2005 - Various lead-free replacements
           - Added Hynix VRAM option and PCBA
05/17/2005 - Added 2 0.1uF caps to VGA sync buffers
05/25/2005 - Added NEC USB2 controller and PCI clock buffer
           - Various lead-free replacements
           - Added pullup to BATT0_DET
05/26/2005 - Removed SMS PIC microcontroller
05/31/2005 - Added 2 8.1uF caps to GPU Vcore output
           - Corrected USB diff pair and spacing/physical rules on ports
06/01/2005 - Corrected caps on FireWire VP rail to 50V
           - Various lead-free replacements
```

DVT

```
06/28/2005 - Added 10K pullup to VIA_REQ_L
           - Changed Q2941 to level shift/pass FET to correct GPU VCore and CPU_Vcore power sequencing
           - Moved R2437 to 3V4_PWRSEQ_L to correct trackpad power state in sleep
           - Moved -FP3V3_SB to RUN rail to correct pumpup problem in sleep
           - Changed to USB1P1-REC BOMOPTION
07/06/2005 - Various lb-free replacements
           - Changed TMDS drive strength resistors to 301 ohm, which was built at EVT
07/08/2005 - Added FET to allow PMU control of trackpad power sequencing
07/09/2005 - Added resistor mux for I2'S MAXBUS I/O rail (PWRON VS RUN)
           - Changed CPU Vcore to 2-states only (no MUX)
           - Removed I2'S connection to TBEN (leakage path)
           - Changed 32.768kHz crystal to new APM specifing 1uW drive parts
           - Added line width constraints to LTC1625 and CPU_Vcore gate nodes
07/14/2005 - Added external 1K pullups in parallel with all I2 internal pullups
07/18/2005 - Changed NEC USB2 series R value to 39.2 ohm
           - Added 150 ohm pulldowns to FW_CTL lines at Vesta
           - Changed TMDS transmitter ferrites to part with higher current rating (1.5A)
           - Added BOMOPTIONS for and stuffed CPU Vcore at 1.28V and 1.30V
07/19/2005 - Added audio mute sequencing FETs
           - Moved DATA DS100BE cap to other side of series resistor
           - Released as REV 05 for DVT
07/22/2005 - Changed all external I2 GPIO pullups to 10K
           - Stuffed R2452, R2482, R2453 to correct I2 2.5V pullup problem
           - Released as REV 04 for DVT
07/25/2005 - Replaced 371S0299 with 371S0300
           - Changed I2 MAXBUS 330HM and I2 MAXBUS 50OHM BOMOPTIONs
           - Changed to Vesta v1.4 as primary U8500, Vesta v1.3 as alternate
07/26/2005 - Changed MCI ADA output series term to 22 ohms
           - Swapped locations (vs. values) of C2500 and C2501
07/29/2005 - Released as REV 05 for DVT
08/03/2005 - Added R3476 on CPU0_TXT_QUAL 10K pulldown.
           - Added R3065 on CPU0_TXC_TCK 10K pull down (no stuff).
           - Changed C1724 and C2285 to 5200pF.
           - Changed C1730 to 5.6pF.
           - Changed C1700 and C1701 and C2215 and C2216 to 47uF.
           - Changed R1720 and R2205 to 7.5K.
           - Released as REV 06 for DVT
```

Pre-PVT

```
08/16/2005 - Replaced C3940-C3947 with ceramic caps
08/17/2005 - Changed power supply solder jumpers to shorts
           - Added five ceramic caps to Vcore supply input
           - Changed D1400,D1401 to 60V schottky to reduce reverse leakage
08/18/2005 - Changed R2958 to 10K to improve power sequencing timing
08/22/2005 - Added FETs to control leakage on Vesta rails.
08/24/2005 - Changed C8600-C8603 to 1uF due to FET isolation
           - Changed R5922 to 100K for power sequencing improvements
           - NO STUFFed R2969 for power sequencing improvements
           - Released as REV 07 for Pre-PVT
```

PVT

```
08/29/2005 - Released as REV A for PVT/Production
09/02/2005 - Stuffed R8420 with 10K, 5% to ensure MDIO logic levels
           - Stuffed R2464 to correct unused GPIO logic level
```

E

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 5 OF 115	

I2S Series Rs

MAKE_BASE=TRUE	22	I2S0_SB_TO_DEV_DTO_R	=RP1150P1	11	11	=RP1150P8	I2S0_SB_TO_DEV_DTO	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_BITCLK_R	=RP1150P2	11	11	=RP1150P7	I2S0_BITCLK	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_MCLK_R	=RP1150P3	11	11	=RP1150P6	I2S0_MCLK	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_SYNC_R	=RP1150P4	11	11	=RP1150P5	I2S0_SYNC	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_SB_TO_DEV_DTO_R	=RP1151P1	11	11	=RP1151P8	I2S1_SB_TO_DEV_DTO	30	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_SYNC_R	=RP1151P2	11	11	=RP1151P7	I2S1_SYNC	30	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_MCLK_R	=RP1151P3	11	11	=RP1151P6	I2S1_MCLK	30	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_BITCLK_R	=RP1151P4	11	11	=RP1151P5	I2S1_BITCLK	30	MAKE_BASE=TRUE

UATA Series Rs

MAKE_BASE=TRUE	63	UATA_DD_R<12>	=RP8150P1	63	63	=RP8150P8	UATA_DD<12>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_CS0_L_R	=RP8150P2	63	63	=RP8150P7	UATA_CS0_L	7 63 64	MAKE_BASE=TRUE	(IDE_CS1FX_L)
MAKE_BASE=TRUE	63	UATA_DD_R<14>	=RP8150P3	63	63	=RP8150P6	UATA_DD<14>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<11>	=RP8150P4	63	63	=RP8150P5	UATA_DD<11>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<7>	=RP8151P1	63	63	=RP8151P8	UATA_DD<7>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<2>	=RP8151P2	63	63	=RP8151P7	UATA_DD<2>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<3>	=RP8151P3	63	63	=RP8151P6	UATA_DD<3>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<15>	=RP8151P4	63	63	=RP8151P5	UATA_DD<15>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<9>	=RP8152P1	63	63	=RP8152P8	UATA_DD<9>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<4>	=RP8152P2	63	63	=RP8152P7	UATA_DD<4>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<6>	=RP8152P3	63	63	=RP8152P6	UATA_DD<6>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<5>	=RP8152P4	63	63	=RP8152P5	UATA_DD<5>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DA_R<2>	=RP8153P1	63	63	=RP8153P8	UATA_DA<2>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<8>	=RP8153P2	63	63	=RP8153P7	UATA_DD<8>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<10>	=RP8153P3	63	63	=RP8153P6	UATA_DD<10>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DA_R<0>	=RP8153P4	63	63	=RP8153P5	UATA_DA<0>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<13>	=RP8154P1	63	63	=RP8154P8	UATA_DD<13>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<0>	=RP8154P2	63	63	=RP8154P7	UATA_DD<0>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DD_R<1>	=RP8154P3	63	63	=RP8154P6	UATA_DD<1>	7 63 64	MAKE_BASE=TRUE	
MAKE_BASE=TRUE	63	UATA_DA_R<1>	=RP8154P4	63	63	=RP8154P5	UATA_DA<1>	7 63 64	MAKE_BASE=TRUE	

Lower DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVOD_R<0>	=RP6720P1	54	54	=RP6720P8	GPU_DVOD<0>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<1>	=RP6720P2	54	54	=RP6720P7	GPU_DVOD<1>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<2>	=RP6720P3	54	54	=RP6720P6	GPU_DVOD<2>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<3>	=RP6720P4	54	54	=RP6720P5	GPU_DVOD<3>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<11>	=RP6721P1	54	54	=RP6721P8	GPU_DVOD<11>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<10>	=RP6721P2	54	54	=RP6721P7	GPU_DVOD<10>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<9>	=RP6721P3	54	54	=RP6721P6	GPU_DVOD<9>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<8>	=RP6721P4	54	54	=RP6721P5	GPU_DVOD<8>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<6>	=RP6722P1	54	54	=RP6722P8	GPU_DVOD<6>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<4>	=RP6722P2	54	54	=RP6722P7	GPU_DVOD<4>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<7>	=RP6722P3	54	54	=RP6722P6	GPU_DVOD<7>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<5>	=RP6722P4	54	54	=RP6722P5	GPU_DVOD<5>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_HSYNC_R	=RP6723P1	54	54	=RP6723P8	GPU_DVO_HSYNC	54 55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_VSYNC_R	=RP6723P2	54	54	=RP6723P7	GPU_DVO_VSYNC	54 55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_DE_R	=RP6723P3	54	54	=RP6723P6	GPU_DVO_DE	54 55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_CLKP_R	=RP6723P4	54	54	=RP6723P5	GPU_DVO_CLKP	54 55	MAKE_BASE=TRUE

Upper DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVOD_R<13>	=RP6821P1	55	55	=RP6821P8	GPU_DVOD<13>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<12>	=RP6821P2	55	55	=RP6821P7	GPU_DVOD<12>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<14>	=RP6821P3	55	55	=RP6821P6	GPU_DVOD<14>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<15>	=RP6821P4	55	55	=RP6821P5	GPU_DVOD<15>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<18>	=RP6822P1	55	55	=RP6822P8	GPU_DVOD<18>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<19>	=RP6822P2	55	55	=RP6822P7	GPU_DVOD<19>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<16>	=RP6822P3	55	55	=RP6822P6	GPU_DVOD<16>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<17>	=RP6822P4	55	55	=RP6822P5	GPU_DVOD<17>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<21>	=RP6823P1	55	55	=RP6823P8	GPU_DVOD<21>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<20>	=RP6823P2	55	55	=RP6823P7	GPU_DVOD<20>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<23>	=RP6823P3	55	55	=RP6823P6	GPU_DVOD<23>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<22>	=RP6823P4	55	55	=RP6823P5	GPU_DVOD<22>	55	MAKE_BASE=TRUE

MAXBUS Pullups

MAKE_BASE=TRUE	33 32	MAXBUS_TS_L	=RP3510P1	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BG_L	=RP3510P2	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_DBG_L	=RP3510P3	32
MAKE_BASE=TRUE		NC_MAXBUS_TBEN_I2 NO_TEST=YES	=RP3510P4	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_BG_L	=RP3511P1	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_HIT_L	=RP3511P2	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_HIT_L	=RP3511P3	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_BR_L	=RP3511P4	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BR_L	=RP3512P1	32
MAKE_BASE=TRUE	33 32	MAXBUS_TA_L	=RP3512P2	32
MAKE_BASE=TRUE	34 32	MAXBUS_CPU0_INT_L	=RP3512P3	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_INT_L	=RP3512P4	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_DRDY_L	=RP3513P2	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DRDY_L	=RP3513P3	32
MAKE_BASE=TRUE	33 32	MAXBUS_AACK_L	=RP3513P4	32
MAKE_BASE=TRUE	33 32	MAXBUS_ARTRY_L	=RP3514P1	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DBG_L	=RP3514P2	32
MAKE_BASE=TRUE	33 32	MAXBUS_TEA_L	=RP3514P3	32

AGP Pullups

MAKE_BASE=TRUE	44 43	AGP_TRDY_L	=RP5610P1	43
MAKE_BASE=TRUE	44 43	AGP_IRDY_L	=RP5610P2	43
MAKE_BASE=TRUE	44 43	AGP_REQ_L	=RP5610P3	43
MAKE_BASE=TRUE	44 43	AGP_RBF_L	=RP5610P4	43
MAKE_BASE=TRUE	44 43	AGP_FRAME_L	=RP5611P1	43
MAKE_BASE=TRUE	44 43	AGP_DEVSEL_L	=RP5611P2	43
MAKE_BASE=TRUE	44 43	AGP_STOP_L	=RP5611P3	43
MAKE_BASE=TRUE	44 43	AGP_GNT_L	=RP5611P4	43

PCI Pullups

MAKE_BASE=TRUE	11	PCI_AIRPORT_GNT_L	=RP7250P1	59
MAKE_BASE=TRUE	60 59 62 61	PCI_TRDY_L	=RP7250P2	59
MAKE_BASE=TRUE	60 59 62 61	PCI_IRDY_L	=RP7250P3	59
MAKE_BASE=TRUE	60 59 62 61	PCI_STOP_L	=RP7250P4	59
MAKE_BASE=TRUE	11	PCI_CBUS_REQ_L	=RP7251P1	59
MAKE_BASE=TRUE	11	PCI_AIRPORT_REQ_L	=RP7251P2	59
MAKE_BASE=TRUE	11	PCI_CBUS_GNT_L	=RP7251P3	59
MAKE_BASE=TRUE	60 59 62 61	PCI_FRAME_L	=RP7251P4	59

USB Pulldowns

72	=RP9210P8	USB2_I2_LEFT_PORT_P	11	MAKE_BASE=TRUE
72	=RP9210P7	USB2_I2_LEFT_PORT_N	11	MAKE_BASE=TRUE
72	=RP9210P6	USB2_I2_P<1>	72	MAKE_BASE=TRUE
72	=RP9210P5	USB2_I2_N<1>	72	MAKE_BASE=TRUE
72	=RP9211P8	USB2_I2_RIGHT_PORT_P	11	MAKE_BASE=TRUE
72	=RP9211P7	USB2_I2_RIGHT_PORT_N	11	MAKE_BASE=TRUE
72	=RP9211P6	USB2_I2_P<3>	72	MAKE_BASE=TRUE
72	=RP9211P5	USB2_I2_N<3>	72	MAKE_BASE=TRUE
72	=RP9212P8	USB_I2_BT_P	11	MAKE_BASE=TRUE
72	=RP9212P7	USB_I2_BT_N	11	MAKE_BASE=TRUE
72	=RP9212P6	USB_I2_TPAD_P	11	MAKE_BASE=TRUE
72	=RP9212P5	USB_I2_TPAD_N	11	MAKE_BASE=TRUE
73	=RP9300P8	USB2_NEC_LEFT_PORT_P	11	MAKE_BASE=TRUE
73	=RP9300P7	USB2_NEC_LEFT_PORT_N	11	MAKE_BASE=TRUE
73	=RP9300P6	USB2_NEC_RIGHT_PORT_N	11	MAKE_BASE=TRUE
73	=RP9300P5	USB2_NEC_RIGHT_PORT_P	11	MAKE_BASE=TRUE
73	=RP9301P8	USB_NEC_BT_P	11	MAKE_BASE=TRUE
73	=RP9301P7	USB_NEC_BT_N	11	MAKE_BASE=TRUE
73	=RP9301P6	USB_NEC_TPAD_N	11	MAKE_BASE=TRUE
73	=RP9301P5	USB_NEC_TPAD_P	11	MAKE_BASE=TRUE

FW Series Rs

MAKE_BASE=TRUE	68 9	FW_D_R<3>	=RP9100P1	71	71	=RP9100P8	FW_D<3>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<1>	=RP9100P2	71	71	=RP9100P7	FW_D<1>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<0>	=RP9100P3	71	71	=RP9100P6	FW_D<0>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<2>	=RP9100P4	71	71	=RP9100P5	FW_D<2>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<7>	=RP9101P1	71	71	=RP9101P8	FW_D<7>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<5>	=RP9101P2	71	71	=RP9101P7	FW_D<5>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<6>	=RP9101P3	71	71	=RP9101P6	FW_D<6>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<4>	=RP9101P4	71	71	=RP9101P5	FW_D<4>	9 69	MAKE_BASE=TRUE

Q41C Pin Swaps

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE D | DRAWING NUMBER 051-6839 | REV. E

SCALE NONE | SHT 6 OF 115

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

POWER	TP12	PP24V_ADAPTER	10	FUNC_TEST=YES
	TP1	PP24V_ALL_PBUSA	10	FUNC_TEST=YES
	TP2	PP12V8_ALL_PBUSB	10	FUNC_TEST=YES
	TP4	PPVCORE_RUN_GPU	10	FUNC_TEST=YES
	TP3	PPVCORE_RUN_CPU	10	FUNC_TEST=YES
	TP6	PP1V8_PWRON	10	FUNC_TEST=YES
	TP5	PP2V5_PWRON	10	FUNC_TEST=YES
	TP7	PP5V_PWRON	10	FUNC_TEST=YES
	TP8	PP3V3_PWRON	10	FUNC_TEST=YES
	TP9	PP5V_RUN	10	FUNC_TEST=YES
	TP10	PP3V3_ALL	10	FUNC_TEST=YES
	TP62	=FTP_GND	7 10	FUNC_TEST=YES

Place 2 TPs @ connector

Place within 50 mm of power supply.

Place 5-10 GND TPs.

LVDS	TP79	LVDS_U0_P	53 56	FUNC_TEST=YES
	TP80	LVDS_U0_N	53 56	FUNC_TEST=YES
	TP81	LVDS_U1_P	53 56	FUNC_TEST=YES
	TP82	LVDS_U1_N	53 56	FUNC_TEST=YES
	TP83	LVDS_U2_P	53 56	FUNC_TEST=YES
	TP84	LVDS_U2_N	53 56	FUNC_TEST=YES
	TP85	CLKLVDS_U_P	53 56	FUNC_TEST=YES
	TP86	CLKLVDS_U_N	53 56	FUNC_TEST=YES
	TP11	LVDS_L0_P	53 56	FUNC_TEST=YES
	TP12	LVDS_L0_N	53 56	FUNC_TEST=YES
	TP13	LVDS_L1_P	53 56	FUNC_TEST=YES
	TP14	LVDS_L1_N	53 56	FUNC_TEST=YES
	TP16	LVDS_L2_P	53 56	FUNC_TEST=YES
	TP15	LVDS_L2_N	53 56	FUNC_TEST=YES
	TP17	CLKLVDS_L_P	53 56	FUNC_TEST=YES
	TP18	CLKLVDS_L_N	53 56	FUNC_TEST=YES
	TP19	LVDS_DDC_CLK	51 56	FUNC_TEST=YES
	TP20	LVDS_DDC_DATA	51 56	FUNC_TEST=YES
	TP21	=PP3V3_DDC_LCD	10 56	FUNC_TEST=YES
	TP63	PP3V3_LCD_CONN	56	FUNC_TEST=YES

Place within 25 mm of LVDS connector.

INVERTER	TP22	PPBUS_INVERTER	56	FUNC_TEST=YES
	TP23	PP5V_INV_SW	56	FUNC_TEST=YES
	TP25	BRIGHT_PWM	56	FUNC_TEST=YES
	TP24	GND_INVERTER	56	FUNC_TEST=YES

Place within 25 mm of inverter connector.

UATA	TP106	=PP5V_RUN_ODD	10 64	FUNC_TEST=YES
	TP117	=PP5V_RUN_HDD	10 64	FUNC_TEST=YES
	TP118	PP3V3R5V_RUN_HDD_LOGIC	64	FUNC_TEST=YES
	TP32	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES
	TP33	UATA_DMARQ	63 64	FUNC_TEST=YES
	TP35	UATA_DSTROBE	63 64	FUNC_TEST=YES
	TP34	UATA_DMACK_L	63 64	FUNC_TEST=YES
	TP36	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES
	TP38	UATA_CS0_L	6 63 64	FUNC_TEST=YES
	TP37	UATA_CS1_L	63 64	FUNC_TEST=YES
	TP40	UATA_RESET_L	63 64	FUNC_TEST=YES
	TP39	UATA_HSTROBE	63 64	FUNC_TEST=YES
	TP41	UATA_STOP	63 64	FUNC_TEST=YES
	TP42	UATA_INTRQ	63 64	FUNC_TEST=YES

Place within 50 mm of ODD/HDD connector.

AUDIO	TP76	PP5V_PWRON_AUDIO_PVDD	74	FUNC_TEST=YES
	TP60	PP5V_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES
	TP59	PP3V3_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES
	TP61	=PP3V3_RUN_AUDIO	10 74	FUNC_TEST=YES
	TP44	=I2C_AUDIO_SCL	8 74	FUNC_TEST=YES
	TP46	=I2C_AUDIO_SDA	8 74	FUNC_TEST=YES
	TP48	I2S0_MCLK	6 74	FUNC_TEST=YES
	TP47	I2S0_BITCLK	6 74	FUNC_TEST=YES
	TP50	I2S0_SYNC	6 74	FUNC_TEST=YES
	TP49	I2S0_SB_TO_DEV_DTO	6 74	FUNC_TEST=YES
	TP51	I2S0_DEV_TO_SB_DTI	22 74	FUNC_TEST=YES
	TP53	AUDIO_LO_MUTE_L	22 74	FUNC_TEST=YES
	TP52	AUDIO_SPKR_MUTE_L	22 74	FUNC_TEST=YES
	TP56	AUDIO_CODEC_RESET_L	22 74	FUNC_TEST=YES
	TP55	AUDIO_SPDIFRX_RESET_L	22 74	FUNC_TEST=YES
	TP57	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES
	TP58	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES
	TP107	AUDIO_LO_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES
	TP108	AUDIO_LI_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES
	TP109	AUDIO_I2S_DTIB_SEL	22 74	FUNC_TEST=YES
	TP110	AUDIO_EXT_MCLK_SEL	22 74	FUNC_TEST=YES
	TP111	AUDIO_GPIO_11	22 74	FUNC_TEST=YES
	TP112	GND_AUDIO_AGND	74	FUNC_TEST=YES
	TP113	GND_AUDIO_PGND	74	FUNC_TEST=YES

Place within 25 mm of audio connector.

SYSTEM	TP76	PP5V_TPAD_F	30	FUNC_TEST=YES
	TP77	USB_TPAD_P	11 30	FUNC_TEST=YES
	TP78	USB_TPAD_N	11 30	FUNC_TEST=YES
	TP88	PP3V3_PWRON_DS1775_R	30	FUNC_TEST=YES
	TP89	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES
	TP43	PP3V3_ALL_HALL_EFFECT_R	30	FUNC_TEST=YES
	TP45	SYS_LID_OPEN_F	30	FUNC_TEST=YES
	TP30	SYS_POWER_BUTTON_L_F	30	FUNC_TEST=YES
	TP29	=FTP_SLEEP_LED	74	FUNC_TEST=YES
	TP31	SYS_CHARGE_LED_L	24 31	FUNC_TEST=YES
	TP87	SYS_ADAPTER_ANALOG_AC_DET	12 31	FUNC_TEST=YES
	TP90	KBDLED_ANODE	28 30	FUNC_TEST=YES
	TP91	KBDLED_RETURN	28 30	FUNC_TEST=YES
	TP105	=I2C_DS1775_SDA	8 30	FUNC_TEST=YES
	TP104	=I2C_DS1775_SCL	8 30	FUNC_TEST=YES

Place within 25 mm of TPAD connector.

CPU FAN	TP100	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES
	TP98	FAN1_TACH	27 31	FUNC_TEST=YES
	TP97	FAN1_PWM	27 31	FUNC_TEST=YES
	TP119	=FTP_GND	7 10	FUNC_TEST=YES

Place within 25 mm of fan connector.

GPU FAN	TP102	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES
	TP103	FAN2_TACH	27 31	FUNC_TEST=YES
	TP101	FAN2_PWM	27 31	FUNC_TEST=YES
	TP120	=FTP_GND	7 10	FUNC_TEST=YES

Place within 25 mm of fan connector.

ALS	TP70	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES
	TP68	ALS_0_OUT	25 31	FUNC_TEST=YES
	TP69	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES

Place within 25 mm of ALS connector.

SCCA	TP72	SCCA_RXD	22 24	FUNC_TEST=YES
	TP71	SCCA_TXD_L	22 24	FUNC_TEST=YES

Place within 25 mm of debug connector.

BACKUP BATT	TP73	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES
	TP74	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES

Place within 25 mm of battery connector.

RT USB	TP64	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES
	TP65	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES
	TP66	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES

Place within 25 mm of right USB connector.

LT USB	TP313	=PP5V_PWRON_LEFT_USB	10 31	FUNC_TEST=YES
	TP310	USB2_LEFT_PORT_P	11 31	FUNC_TEST=YES
	TP315	USB2_LEFT_PORT_N	11 31	FUNC_TEST=YES

Place within 25 mm of left USB connector.

Functional Test Points

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
	I2C	I2C		I2C_PMU_SMB_SCL 8
	I2C	I2C		I2C_PMU_SMB_SDA 8
	I2C	I2C		I2C_PMU_SCL 8
	I2C	I2C		I2C_PMU_SDA 8
I2C_NB	I2C	I2C		I2C_I2_NB_SCL 8
I2C_NB	I2C	I2C		I2C_I2_NB_SDA 8
	I2C	I2C		I2C_I2_SB_SCL 8
	I2C	I2C		I2C_I2_SB_SDA 8
	I2C	I2C		I2C_GPU_TMDS_SCL 8
	I2C	I2C		I2C_GPU_TMDS_SDA 8

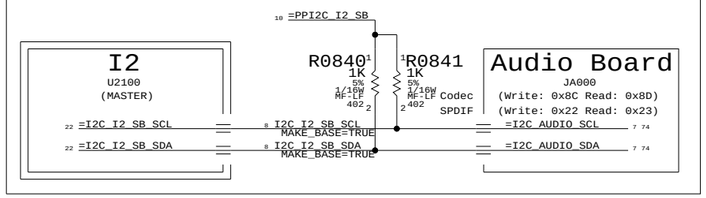
Page Notes

Power aliases required by this page:
(NONE)

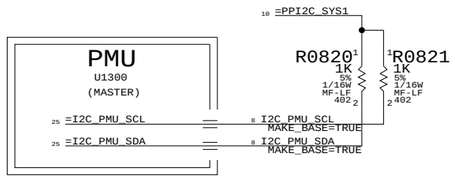
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GOV_I2C / GOV_I2C_BYPASS
  Allows bypassing Governator I2C bus. Most devices are connected directly to PMU unstead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.
- MMM_PWR_ALL / MMM_PWR_PWRON
  Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown. NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.

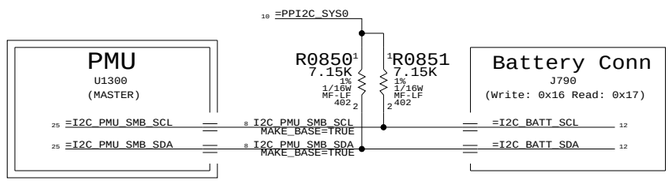
SouthBridge I2C Bus



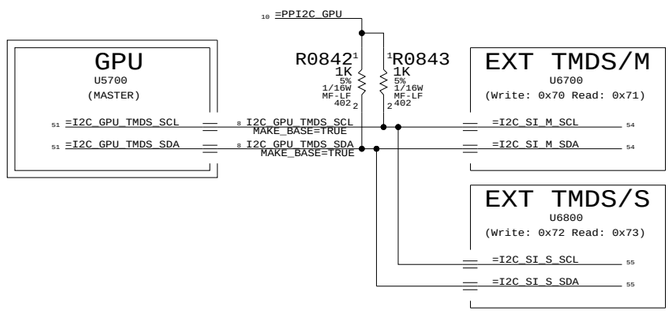
PMU I2C Bus



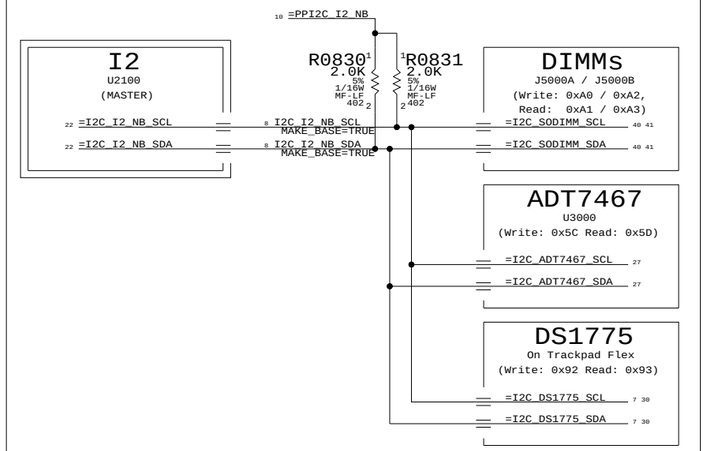
PMU SMBus



GPU I2C Bus



NorthBridge I2C Bus



I2C Connections

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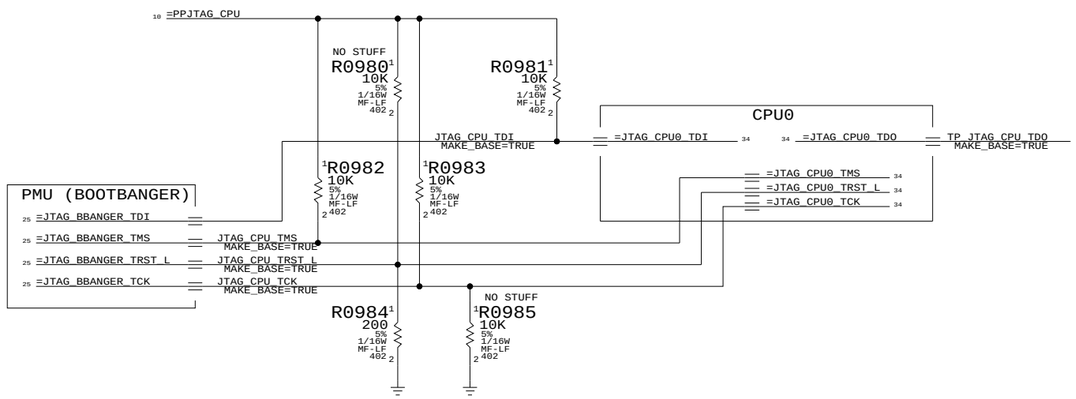
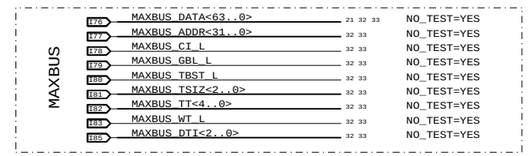
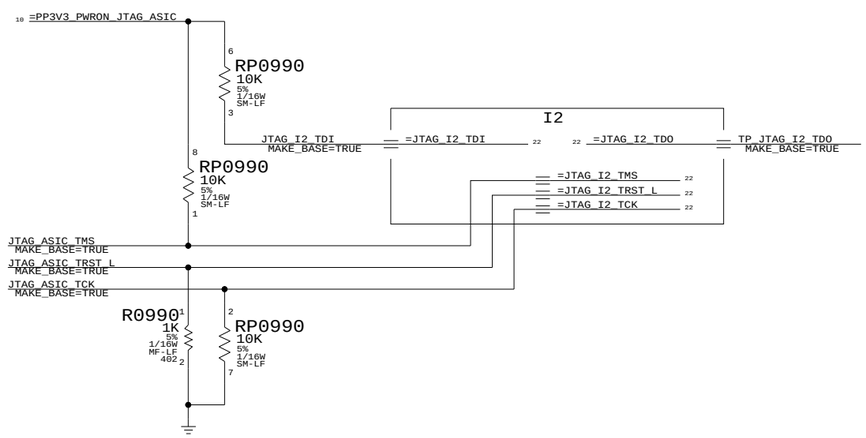
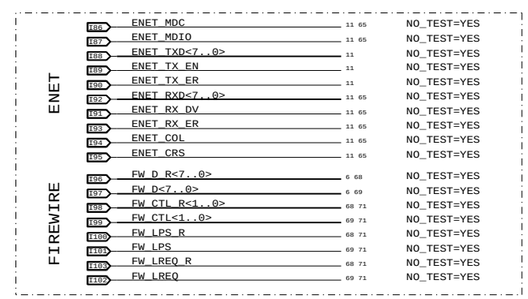
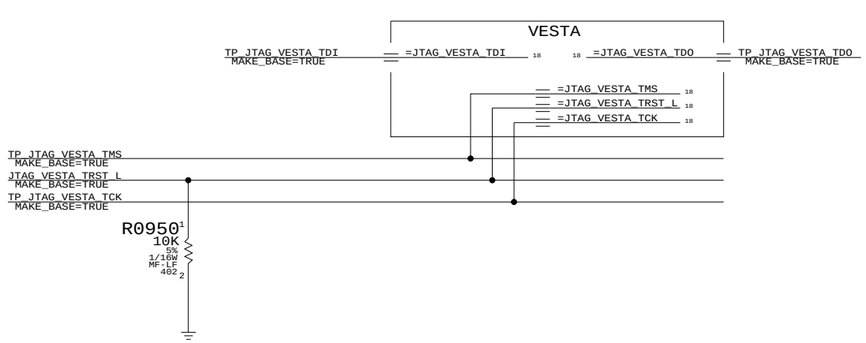


Nets not requiring TPs due to JTAG









JTAG Connections

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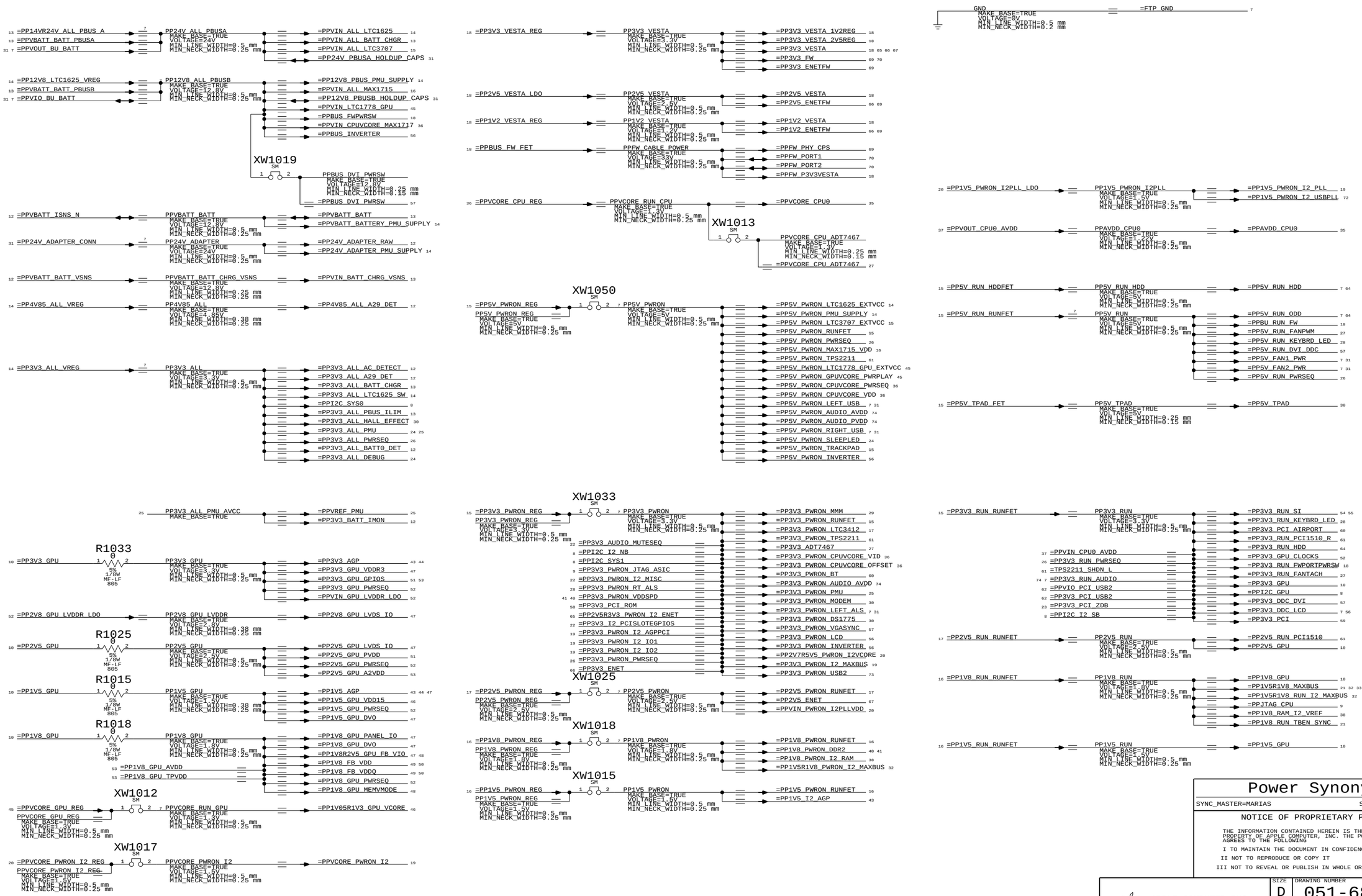

Power Synonyms

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SCALE NONE	SHT 10 OF 115	

I2S0 Series Rs

RP1150 33 5% 1/16W SM-LF

6 =RP1150P1	1	8	=RP1150P8 6
6 =RP1150P2	2	7	=RP1150P7 6
6 =RP1150P3	3	6	=RP1150P6 6
6 =RP1150P4	4	5	=RP1150P5 6

One resistor for each of:
- I2S0_SB_TO_DEV_DTO(_R)
- I2S0_MCLK(_R)
- I2S0_BITCLK(_R)
- I2S0_SYNC(_R)

I2S1 Series Rs

RP1151 33 5% 1/16W SM-LF

6 =RP1151P1	1	8	=RP1151P8 6
6 =RP1151P2	2	7	=RP1151P7 6
6 =RP1151P3	3	6	=RP1151P6 6
6 =RP1151P4	4	5	=RP1151P5 6

One resistor for each of:
- I2S1_SB_TO_DEV_DTO(_R)
- I2S1_MCLK(_R)
- I2S1_BITCLK(_R)
- I2S1_SYNC(_R)

GPU

R1140 22 5% 1/16W MF-LF 402

43 AGP_CLK66M_GPU_R → 1 — 2 → AGP_CLK66M_GPU 44

25 11 PCI_RESET_L — MAKE_BASE=TRUE — =AGP_GPU_RESET_L 44

AGP_VREF — MAKE_BASE=TRUE, VOLTAGE=0.75V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.15 mm
- =I2_AGP_VREF 43
- =AGP_VREF 44
- =GPU_AGP_VREF 44

51 TP_EXTTMDS_RESET_L — SI_TMDS_RESET_L — MAKE_BASE=TRUE — =SI_TMDS_RESET_L 54 55

CPU Clocks

R1110 10 5% 1/16W MF-LF 402

32 MAXBUS_CLK_CPU0_R → 1 — 2 → MAXBUS_CLK_CPU0 — MAKE_BASE=TRUE — =MAXBUS_CPU0_CLK 33

MAXBUS_TBEN_SYNC

R1111 10 5% 1/16W MF-LF 402

32 TP_MAXBUS_CLK_CPU1_R — MAXBUS_CLK_CPU1_R — MAKE_BASE=TRUE → 1 — 2 → MAXBUS_CLK_TBEN_SYNC — MAKE_BASE=TRUE — =SYSCLK_TBEN_SYNC 21

USB Controller Mux

R1160 0 5% 1/16W MF-LF 402 — USB2_NEC — USB2_NEC_LEFT_PORT_P
R1161 0 5% 1/16W MF-LF 402 — USB2_I2 — USB2_I2_LEFT_PORT_P

31 7 USB2_LEFT_PORT_P → 1 — 2 → 6 11
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB2_LT_PORT

R1162 0 5% 1/16W MF-LF 402 — USB2_NEC — USB2_NEC_LEFT_PORT_N
R1163 0 5% 1/16W MF-LF 402 — USB2_I2 — USB2_I2_LEFT_PORT_N

31 7 USB2_LEFT_PORT_N → 1 — 2 → 6 11
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB2_LT_PORT

R1164 0 5% 1/16W MF-LF 402 — USB2_NEC — USB2_NEC_RIGHT_PORT_P
R1165 0 5% 1/16W MF-LF 402 — USB2_I2 — USB2_I2_RIGHT_PORT_P

31 7 USB2_RIGHT_PORT_P → 1 — 2 → 6 11
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB2_RT_PORT

R1166 0 5% 1/16W MF-LF 402 — USB2_NEC — USB2_NEC_RIGHT_PORT_N
R1167 0 5% 1/16W MF-LF 402 — USB2_I2 — USB2_I2_RIGHT_PORT_N

31 7 USB2_RIGHT_PORT_N → 1 — 2 → 6 11
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB2_RT_PORT

R1170 0 5% 1/16W MF-LF 402 — USB1P1_NEC — USB_NEC_BT_P
R1171 0 5% 1/16W MF-LF 402 — USB1P1_I2 — USB_I2_BT_P

60 USB_BT_P → 1 — 2 → 6 11
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB_BT

R1172 0 5% 1/16W MF-LF 402 — USB1P1_NEC — USB_NEC_BT_N
R1173 0 5% 1/16W MF-LF 402 — USB1P1_I2 — USB_I2_BT_N

60 USB_BT_N → 1 — 2 → 6 11
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB_BT

R1174 0 5% 1/16W MF-LF 402 — USB1P1_NEC — USB_NEC_TPAD_P
R1175 0 5% 1/16W MF-LF 402 — USB1P1_I2 — USB_I2_TPAD_P

30 7 USB_TPAD_P → 1 — 2 → 6 11
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB_TPAD

R1176 0 5% 1/16W MF-LF 402 — USB1P1_NEC — USB_NEC_TPAD_N
R1177 0 5% 1/16W MF-LF 402 — USB1P1_I2 — USB_I2_TPAD_N

30 7 USB_TPAD_N → 1 — 2 → 6 11
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB_TPAD

PCI

R1120 22 5% 1/16W MF-LF 402

59 TP_PCI_CLK33M_SLOTA_R — PCI_CLK33M_ZDB_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_ZDB — MAKE_BASE=TRUE — =PCI_CLK33M_ZDB_IN 23

MAXBUS_TBEN_SYNC

R1130 22 5% 1/16W MF-LF 402

59 TP_PCI_CLK33M_SLOTD_R — PCI_CLK33M_TBEN_SYNC_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_TBEN_SYNC — MAKE_BASE=TRUE — =CLK33M_TBEN_SYNC 21

R1135 22 5% 1/16W MF-LF 402

23 =PCI_CLK33M_ZDBOUT_R<0> — PCI_CLK33M_AIRPORT_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_AIRPORT — MAKE_BASE=TRUE — =PCI_CLK33M_AIRPORT 60

59 PCI_SLOTA_REQ_L ← 6 — PCI_AIRPORT_REQ_L — MAKE_BASE=TRUE — =PCI_AIRPORT_REQ_L 60
59 PCI_SLOTA_GNT_L → 6 — PCI_AIRPORT_GNT_L — MAKE_BASE=TRUE — =PCI_AIRPORT_GNT_L 60
59 22 PCI_SLOTA_INT_L ← — PCI_AIRPORT_INT_L — MAKE_BASE=TRUE — =PCI_AIRPORT_INT_L 60
62 61 60 59 58 PCI_AD<17> — MAKE_BASE=TRUE — =PCI_AIRPORT_IDSEL 60
25 11 PCI_RESET_L — MAKE_BASE=TRUE — =PCI_AIRPORT_RESET_L 60

R1136 22 5% 1/16W MF-LF 402

23 =PCI_CLK33M_ZDBOUT_R<1> — PCI_CLK33M_CBUS_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_CBUS — MAKE_BASE=TRUE — =PCI_CLK33M_CBUS 61

59 PCI_SLOTD_REQ_L ← 6 — PCI_CBUS_REQ_L — MAKE_BASE=TRUE — =PCI_CBUS_REQ_L 61
59 PCI_SLOTD_GNT_L → 6 — PCI_CBUS_GNT_L — MAKE_BASE=TRUE — =PCI_CBUS_GNT_L 61
59 22 PCI_SLOTD_INT_L ← — PCI_CBUS_INT_L — MAKE_BASE=TRUE — =PCI_CBUS_INT_L 61
62 61 60 59 58 PCI_AD<20> — MAKE_BASE=TRUE — =PCI_CBUS_IDSEL 61
25 11 PCI_RESET_L — MAKE_BASE=TRUE — =PCI_CBUS_RESET_L 61

R1137 22 5% 1/16W MF-LF 402

23 =PCI_CLK33M_ZDBOUT_R<2> — PCI_CLK33M_USB2_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_USB2 — MAKE_BASE=TRUE — =PCI_CLK33M_USB2 62

22 PCI_SLOTE_REQ_L ← — PCI_USB2_REQ_L — MAKE_BASE=TRUE — =PCI_USB2_REQ_L 62
22 PCI_SLOTE_GNT_L → — PCI_USB2_GNT_L — MAKE_BASE=TRUE — =PCI_USB2_GNT_L 62
22 PCI_SLOTE_INT_L ← — PCI_USB2_INT_L — MAKE_BASE=TRUE — =PCI_USB2_INT_L 62
62 61 60 59 PCI_AD<21> — MAKE_BASE=TRUE — =PCI_USB2_IDSEL 62
25 11 PCI_RESET_L — MAKE_BASE=TRUE — =PCI_USB2_RESET_L 62

23 =PCI_CLK33M_ZDBOUT_R<3> — TP_PCI_CLK33M_ZDBOUT3 — MAKE_BASE=TRUE

USB Port Assignments

11 6 USB2_I2_LEFT_PORT_P — MAKE_BASE=TRUE — USB2_I2_P<0> 72
11 6 USB2_I2_LEFT_PORT_N — MAKE_BASE=TRUE — USB2_I2_N<0> 72
11 6 USB2_I2_RIGHT_PORT_P — MAKE_BASE=TRUE — USB2_I2_P<2> 72
11 6 USB2_I2_RIGHT_PORT_N — MAKE_BASE=TRUE — USB2_I2_N<2> 72
11 6 USB_I2_BT_P — MAKE_BASE=TRUE — USB2_I2_P<4> 72
11 6 USB_I2_BT_N — MAKE_BASE=TRUE — USB2_I2_N<4> 72
11 6 USB_I2_TPAD_P — MAKE_BASE=TRUE — USB2_I2_P<5> 72
11 6 USB_I2_TPAD_N — MAKE_BASE=TRUE — USB2_I2_N<5> 72

11 6 USB2_NEC_LEFT_PORT_P — MAKE_BASE=TRUE — USB2_NEC_P<0> 73
11 6 USB2_NEC_LEFT_PORT_N — MAKE_BASE=TRUE — USB2_NEC_N<0> 73
11 6 USB2_NEC_RIGHT_PORT_P — MAKE_BASE=TRUE — USB2_NEC_P<1> 73
11 6 USB2_NEC_RIGHT_PORT_N — MAKE_BASE=TRUE — USB2_NEC_N<1> 73
11 6 USB_NEC_BT_P — MAKE_BASE=TRUE — USB2_NEC_P<2> 73
11 6 USB_NEC_BT_N — MAKE_BASE=TRUE — USB2_NEC_N<2> 73
11 6 USB_NEC_TPAD_P — MAKE_BASE=TRUE — USB2_NEC_P<3> 73
11 6 USB_NEC_TPAD_N — MAKE_BASE=TRUE — USB2_NEC_N<3> 73

PMU Connections

30 25 7 SYS_OVERTEMP_L — MAKE_BASE=TRUE — =ADT7467_THERM_L 27
13 PMU_CHARGE_V — MAKE_BASE=TRUE — TP_PMU_P7_5 25
25 PMU_CPU_HRESET_L — MAKE_BASE=TRUE — =CPU_HRESET_L 34
12 SYS_PMU_ANALOG_AC_DET — MAKE_BASE=TRUE — TP_PMU_AN_P10_6 25
25 GOV_RESET_L — TP_GOV_RESET_L — MAKE_BASE=TRUE
25 PMU_CPU_CLK_EN — MAKE_BASE=TRUE — =I2_STOPCPU_L 22
25 PMU_SYS_CLK_EN — MAKE_BASE=TRUE — =I2_STOPXTAL_L 22

PM0 TP_PMU_P3_0 — MAKE_BASE=TRUE 25
PM0 TP_PMU_P3_1 — MAKE_BASE=TRUE 25
PM0 TP_PMU_P3_2 — MAKE_BASE=TRUE 25
PM0 TP_PMU_P3_3 — MAKE_BASE=TRUE 25

26 SYS_PWRSEQ_TPAD_L — MAKE_BASE=TRUE — TP_PMU_AN_P0_0 25
26 SYS_PWRSEQ_1 — MAKE_BASE=TRUE — TP_PMU_AN_P0_1 25
26 SYS_PWRSEQ_2 — MAKE_BASE=TRUE — TP_PMU_AN_P0_2 25
26 SYS_PWRSEQ_3_L — MAKE_BASE=TRUE — TP_PMU_AN_P0_3 25
26 SYS_PWRSEQ_4 — MAKE_BASE=TRUE — TP_PMU_AN_P0_4 25
26 SYS_PWRSEQ_5 — MAKE_BASE=TRUE — TP_PMU_AN_P0_5 25
26 SYS_PWRSEQ_6_L — MAKE_BASE=TRUE — TP_PMU_P7_4 25
26 SYS_PWRSEQ_FINAL — MAKE_BASE=TRUE — TP_PMU_AN_P10_5 25

Vesta Ethernet

65 ENET_TX_EN_R → 9 — ENET_TX_EN — MAKE_BASE=TRUE → =ENET_TX_EN 66
65 ENET_TX_ER_R → 9 — ENET_TX_ER — MAKE_BASE=TRUE → =ENET_TX_ER 66
65 ENET_TXD_R<7..0> → 9 — ENET_TXD<7..0> — MAKE_BASE=TRUE → =ENET_TXD<7..0> 66
65 ENET_RESET_L → R1185 100K 5% 1/16W MF-LF 402 2

65 9 ENET_RXD<7..0> — MAKE_BASE=TRUE — =ENET_RXD_R<7..0> 66
65 9 ENET_RX_DV — MAKE_BASE=TRUE — =ENET_RX_DV_R 66
65 9 ENET_RX_ER — MAKE_BASE=TRUE — =ENET_RX_ER_R 66
65 9 ENET_COL — MAKE_BASE=TRUE — =ENET_COL_R 66
65 9 ENET_CRS — MAKE_BASE=TRUE — =ENET_CRS_R 66
65 ENET_CLK125M_GBE_REF — MAKE_BASE=TRUE — =VESTA_CLK125M_GBE_REF 66
65 ENET_CLK125M_RX — MAKE_BASE=TRUE — =VESTA_CLK125M_RX 66
65 ENET_CLK25M_TX — MAKE_BASE=TRUE — =VESTA_CLK25M_TX 66
65 9 ENET_MDC — MAKE_BASE=TRUE — =VESTA_MDC 66
65 9 ENET_MDIO — MAKE_BASE=TRUE — =VESTA_MDIO 66
TP_ENET_ENERGYDET — MAKE_BASE=TRUE — =VESTA_ENERGYDET 66

MISC

25 11 PCI_RESET_L — MAKE_BASE=TRUE — =ROM_PWD_L 58
32 TP_MAXBUS_CPU1_QACK_L — NC_MAXBUS_CPU1_QACK_L — MAKE_BASE=TRUE, NO_TEST=YES

22 I2_GPIO_EXT_02 — CPU0_VID_AB_SEL — MAKE_BASE=TRUE — =CPU0_VID_AB_SEL 36
22 =SPI_I2_REQ — CPU0_MAX1717_AB_SEL — MAKE_BASE=TRUE — =CPU0_MAX1717_AB_SEL 36
24 =SLEEP_LED_IOUT — SLEEP_LED_IOUT — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm — =SLEEP_LED_CONN 74

Signal Synonyms

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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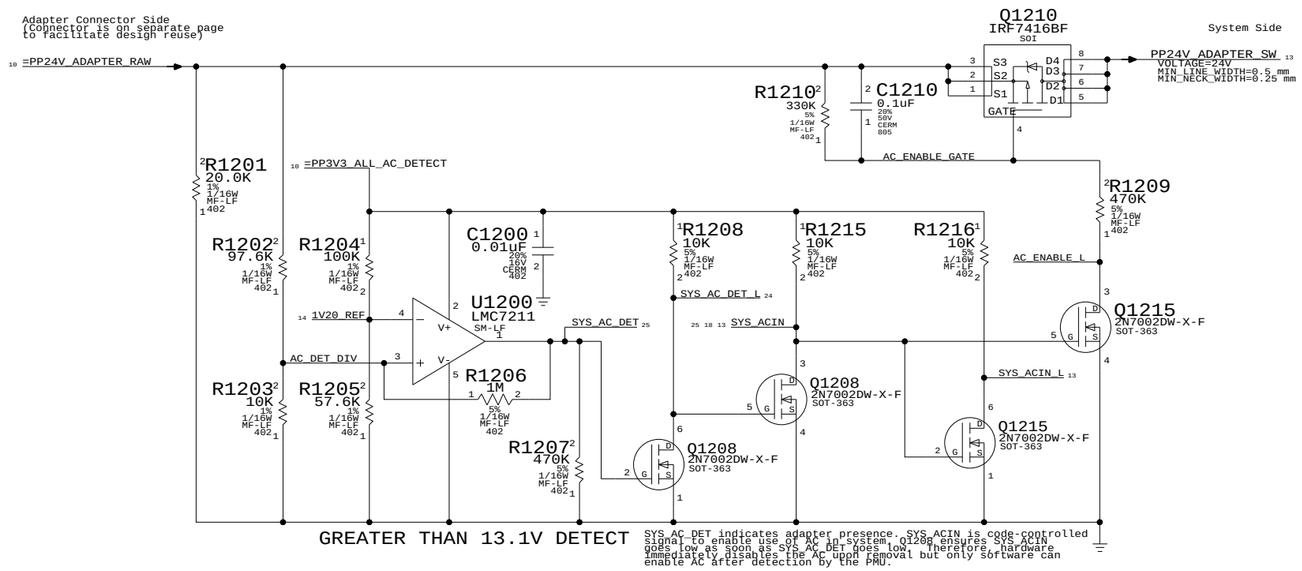
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 11 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
PBA17	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINP 12
PBA18	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINN 12

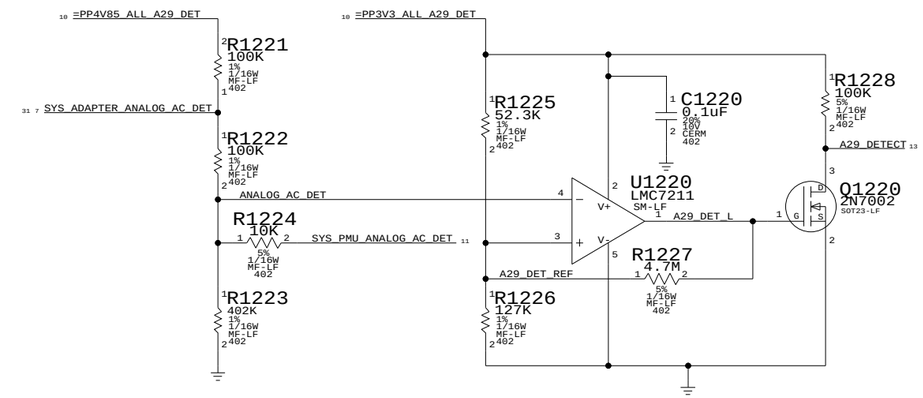
ADAPTER INPUT/INRUSH LIMITER



GREATER THAN 13.1V DETECT

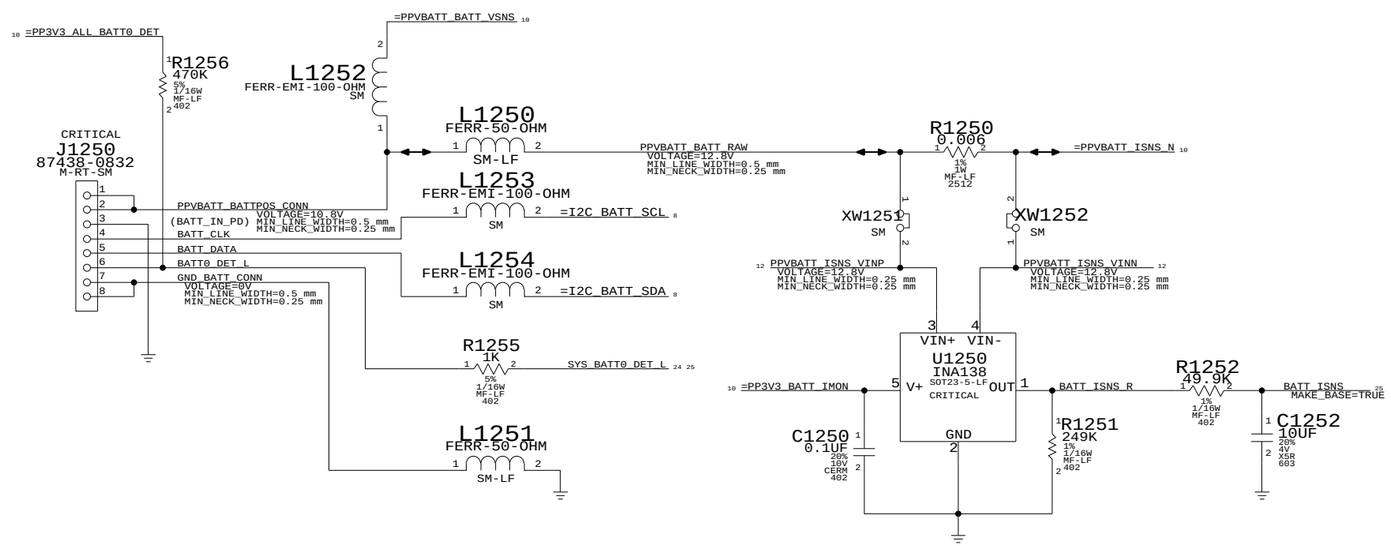
SYS_AC_DET indicates adapter presence. SYS_ACIN is code-controlled signal to enable use of AC in system. Q1208 ensures SYS_ACIN goes low as soon as SYS_AC_DET goes low. Therefore, hardware immediately disables the AC upon removal but only software can enable AC after detection by the PMU.

A29 ADAPTER DETECTION



ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

BATTERY INPUT/CURRENT SENSE



Power Inputs

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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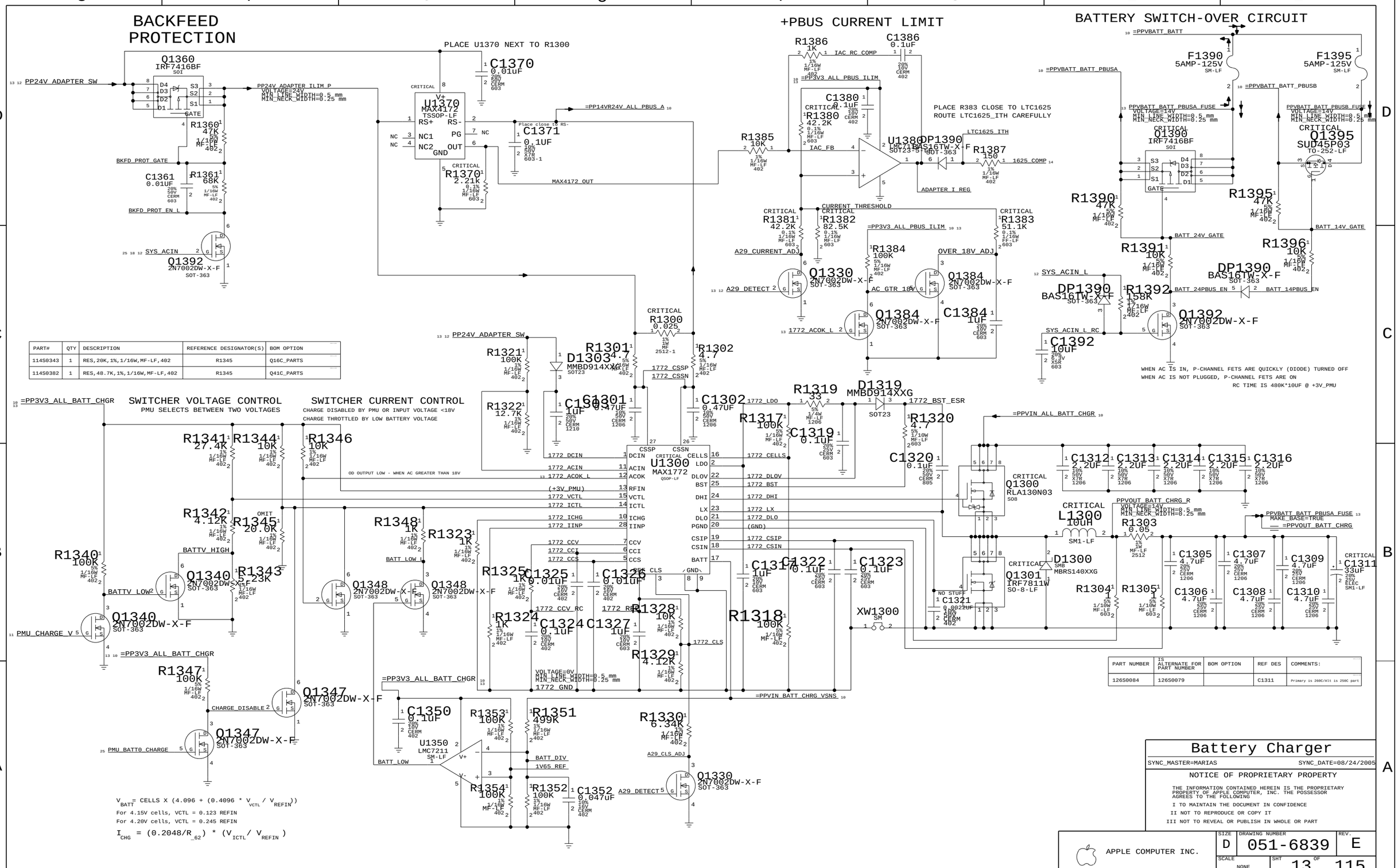


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0343	1	RES,20K,1%,1/16W,MF-LF,402	R1345	Q16C_PARTS
114S0382	1	RES,48.7K,1%,1/16W,MF-LF,402	R1345	Q41C_PARTS

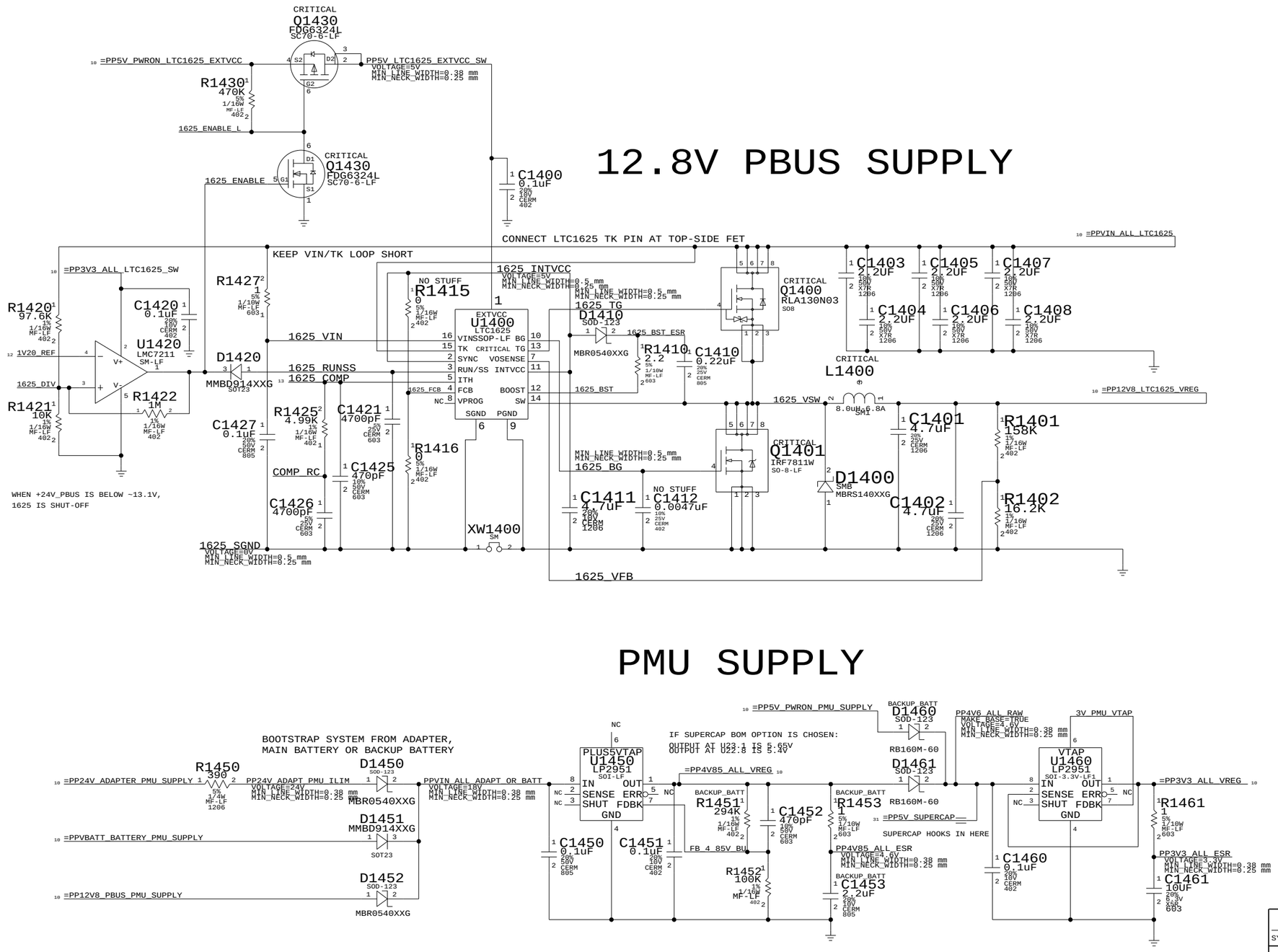
PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0084	126S0079		C1311	Primary is 260C/Alt is 250C part

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0465	1	RES,MF-LF,1/16W,357K OHM,1%,0402,SMD	R1451	?	SUPERCAP

12.8V PBUS/PMU Supplies

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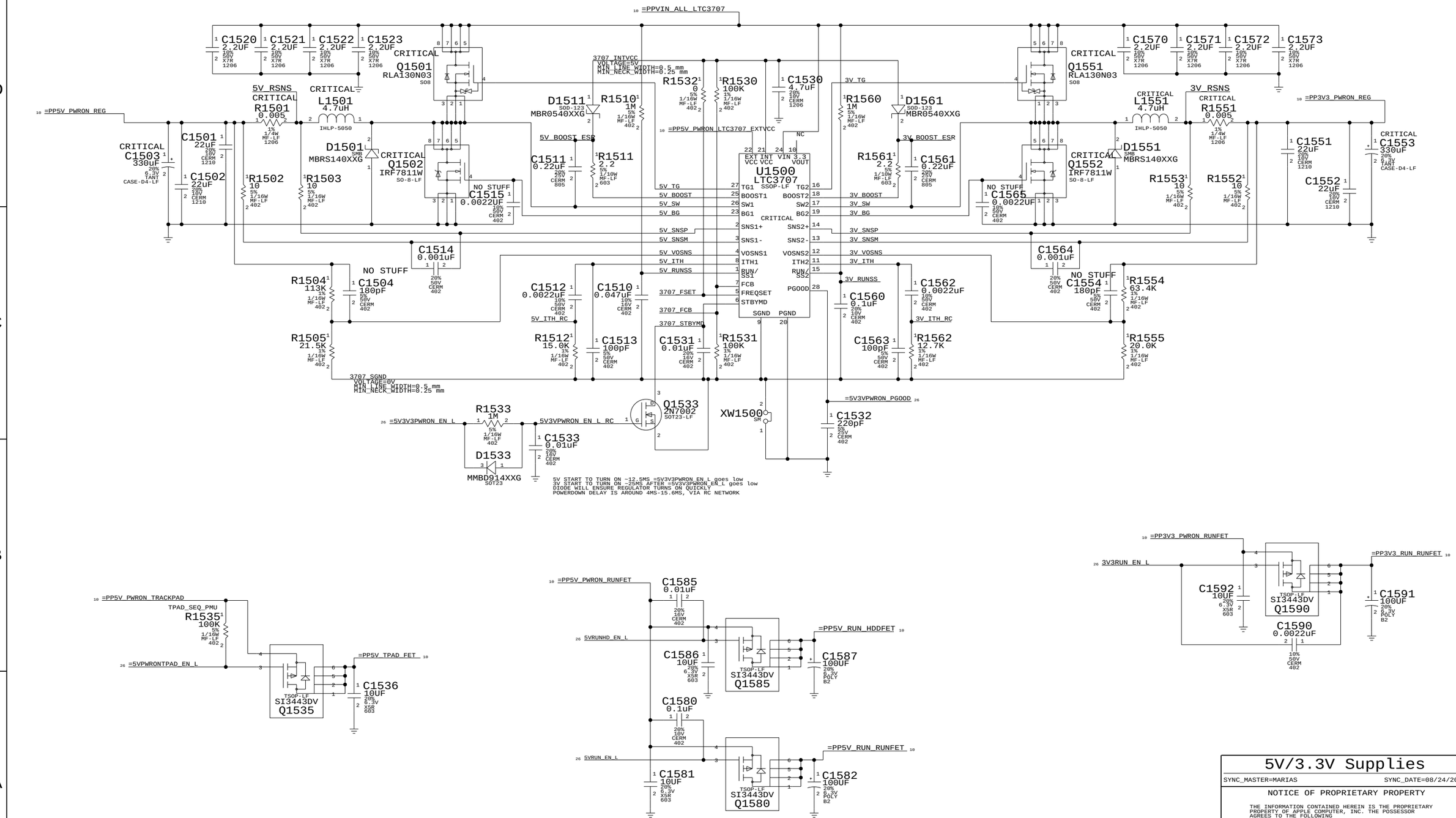
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 14 OF 115	

3.3V/5V SWITCHER



5V/3.3V Supplies

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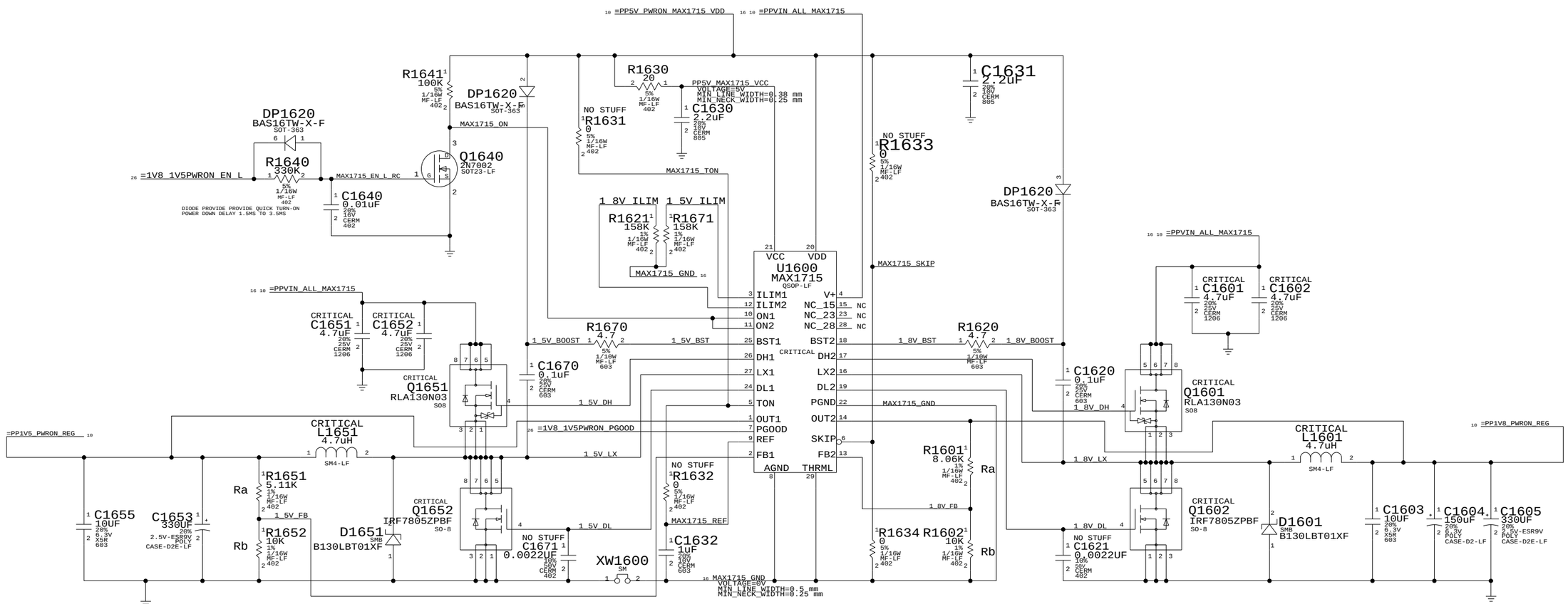
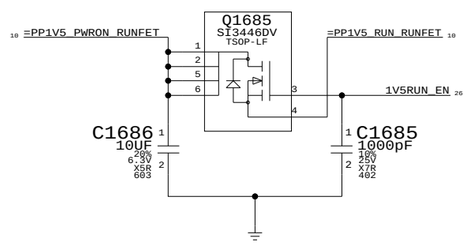
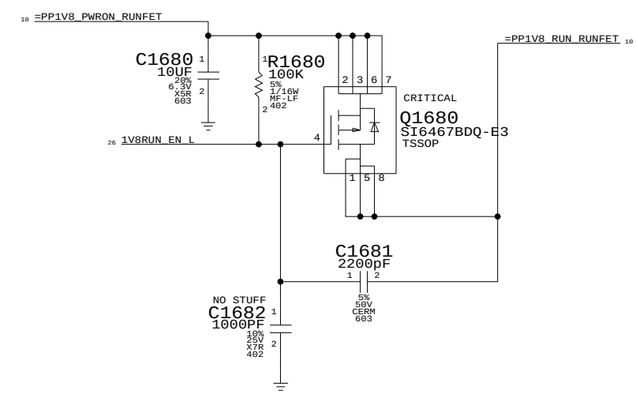
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 15 OF 115	

1.5V/1.8V SWITCHER



Vout = 1.0V * (1 + Ra/Rb)





1.8V/1.5V Supplies

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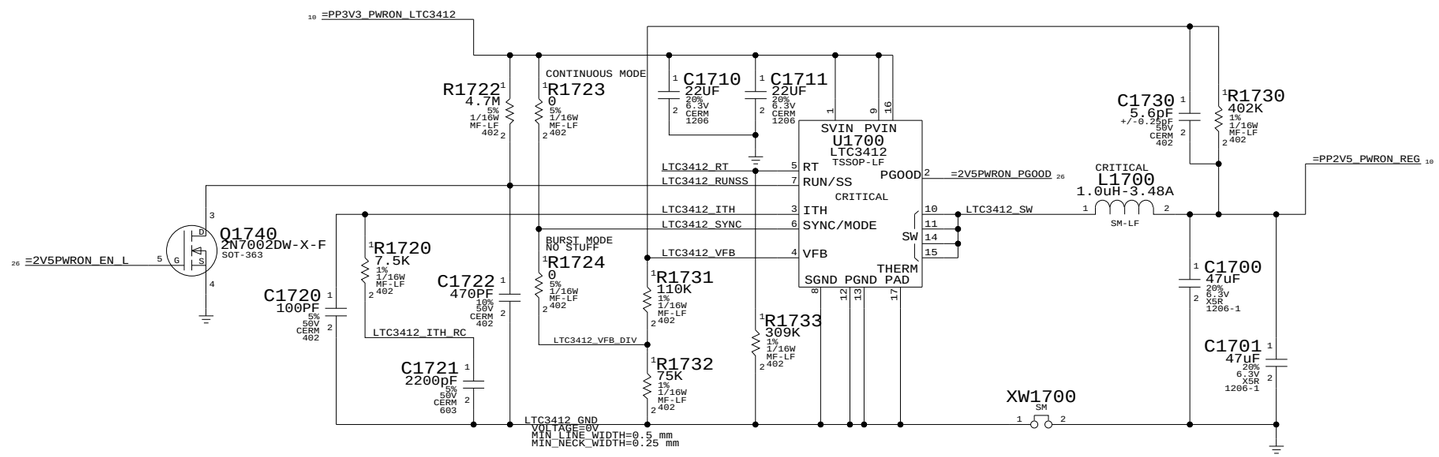
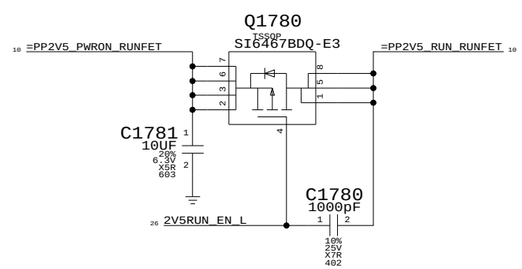
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 16 OF 115	

2.5V SWITCHER





2.5V Supply

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 17 OF 115	

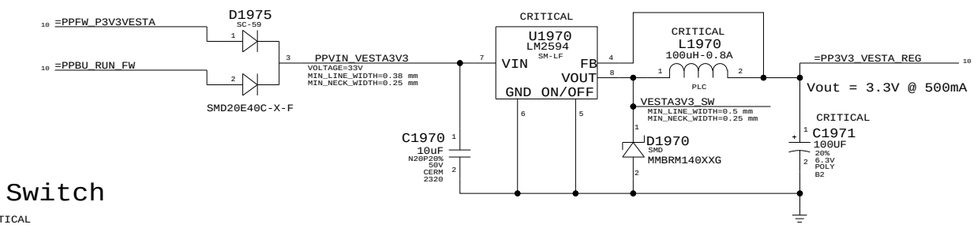
Page Notes

Power aliases required by this page:
- =PPBUS_FW (system supply for bus power)
- =PPBU_RUN_FW (backup PHY power)
- =PP3V3_RUN_FWPORTPWRSW

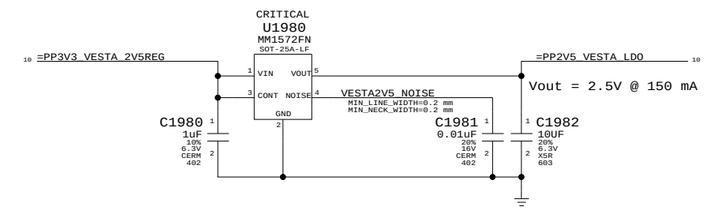
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

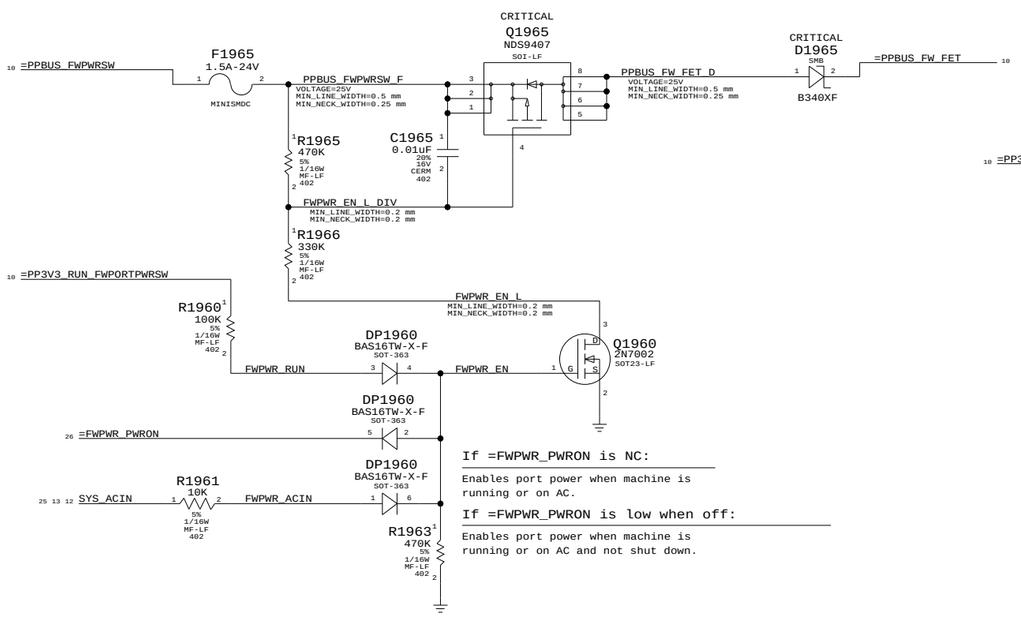
3.3V Regulator



2.5V LDO



Port Power Switch



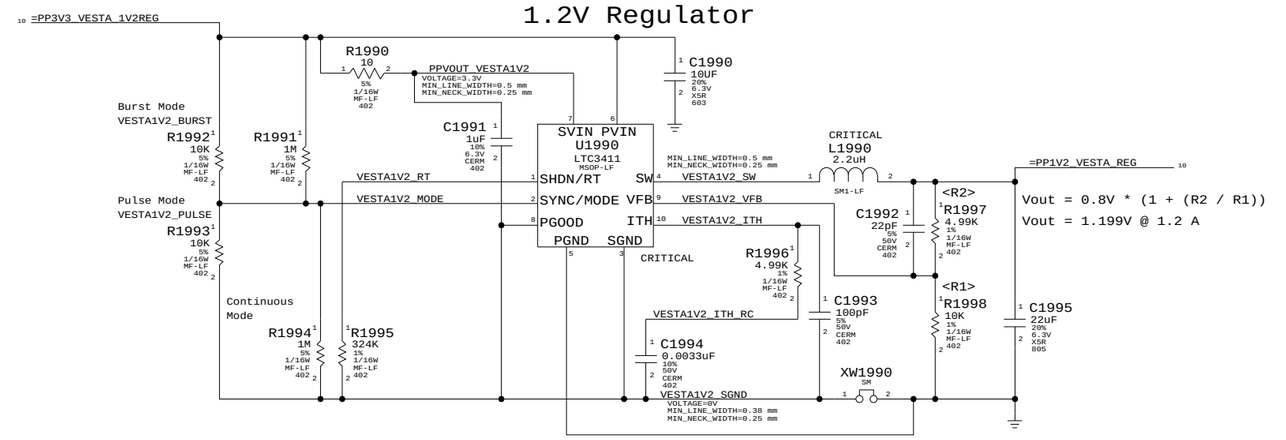
If =FWPWR_PWRON is NC:

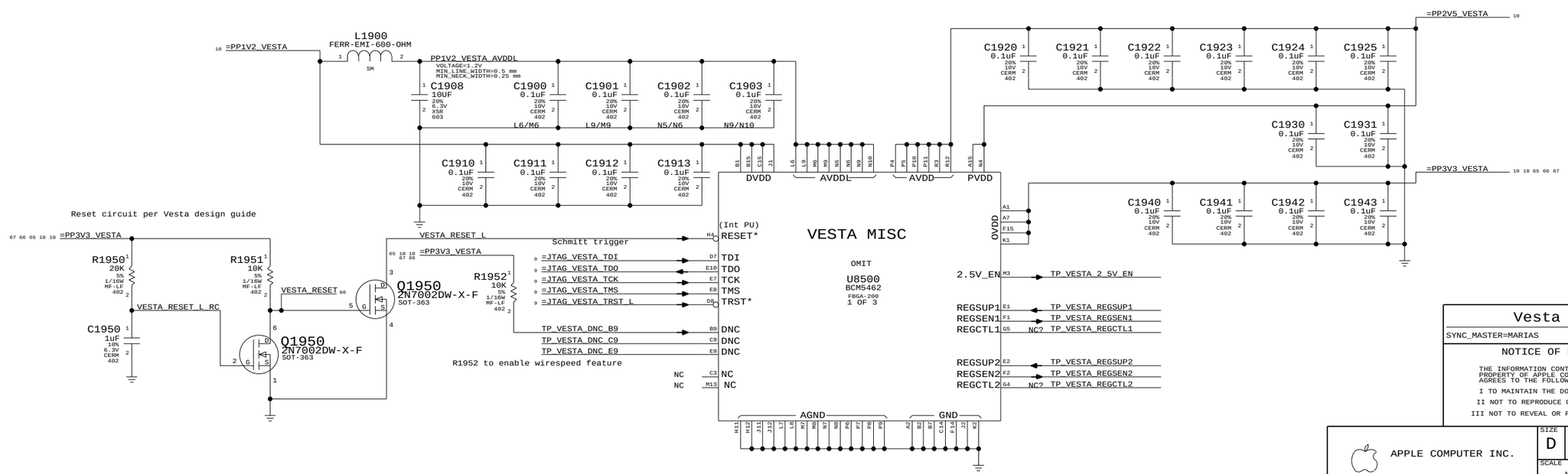
Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:

Enables port power when machine is running or on AC and not shut down.

1.2V Regulator





Vesta Power & Misc

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 19 OF 115	

Page Notes

Power aliases required by this page:
- =PPVCORE_PWRON_I2
- =PP1V5_PWRON_I2_PLL
- =PP3V3_PWRON_I2_IO1
- =PP3V3_PWRON_I2_IO2
- =PP3V3_PWRON_I2_AGPPCI
- =PP3V3_PWRON_I2_MAXBUS

NOTE: The four 3.3V rails are meant to be aliased together. They are called out separately for test purposes.
NOTE: When these four rails are not aliased together, make sure there is at least one 10uF cap per rail.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

VCore Bypassing

(25 Balls on I2)

4 X 10uF (0603)
25 X 1uF (0402)

=PPVCORE_PWRON_I2

C2146 10UF 20% 6.3V X5R 603
C2147 10UF 20% 6.3V X5R 603
C2148 10UF 20% 6.3V X5R 603
C2149 10UF 20% 6.3V X5R 603
C2120 1uF 10% 6.3V CERM 402
C2121 1uF 10% 6.3V CERM 402
C2122 1uF 10% 6.3V CERM 402
C2123 1uF 10% 6.3V CERM 402
C2124 1uF 10% 6.3V CERM 402
C2125 1uF 10% 6.3V CERM 402
C2126 1uF 10% 6.3V CERM 402
C2127 1uF 10% 6.3V CERM 402
C2128 1uF 10% 6.3V CERM 402
C2129 1uF 10% 6.3V CERM 402
C2130 1uF 10% 6.3V CERM 402
C2131 1uF 10% 6.3V CERM 402
C2132 1uF 10% 6.3V CERM 402
C2133 1uF 10% 6.3V CERM 402
C2134 1uF 10% 6.3V CERM 402
C2135 1uF 10% 6.3V CERM 402
C2136 1uF 10% 6.3V CERM 402
C2137 1uF 10% 6.3V CERM 402
C2138 1uF 10% 6.3V CERM 402
C2139 1uF 10% 6.3V CERM 402
C2140 1uF 10% 6.3V CERM 402
C2141 1uF 10% 6.3V CERM 402
C2142 1uF 10% 6.3V CERM 402
C2143 1uF 10% 6.3V CERM 402
C2144 1uF 10% 6.3V CERM 402

3.3V I/O DECOUPLING

(48 Balls on I2)

1 X 10uF (0603)
48 X 1uF (0402)

=PP3V3_PWRON_I2_IO1
=PP3V3_PWRON_I2_IO2
=PP3V3_PWRON_I2_MAXBUS
=PP3V3_PWRON_I2_AGPPCI

C2150 C2151 C2152 C2153 C2154 C2155 C2156 C2157 C2158 C2159 C2160 C2161 C2162 C2163 C2164 C2165 C2166 C2167 C2168 C2169 C2170 C2171 C2172 C2173 C2174 C2175 C2176 C2177 C2178 C2179 C2180 C2181 C2182 C2183 C2184 C2185 C2186 C2187 C2188 C2189 C2190 C2191 C2192 C2193 C2194 C2195 C2196 C2197
1uF 10% 6.3V CERM 402

C2199 10UF 20% 6.3V X5R 603

OMIT
U2100
I2
BGA
3.3V I/O POWER
(2 of 14)

VDD33_AGP: VDD33_0 (AH17)
VDD33_1 (E3), VDD33_2 (F5), VDD33_3 (H3), VDD33_4 (H6), VDD33_5 (J8), VDD33_6 (L10), VDD33_7 (L3), VDD33_8 (L6), VDD33_9 (N13), VDD33_10 (P12), VDD33_11 (P3), VDD33_12 (P6), VDD33_13 (R14), VDD33_14 (T13)
For USB, Firewire, I2S and some GPIOs — VDD33_IO_1 (14)
VDD33_15 (AB13), VDD33_16 (AC15), VDD33_17 (AC3), VDD33_18 (AC6), VDD33_19 (AF11), VDD33_20 (AF3), VDD33_21 (AF6), VDD33_22 (AF9), VDD33_23 (AJ3), VDD33_24 (AJ6), VDD33_25 (AM3), VDD33_26 (Y13)
For GPIOs, Pwr Mgt — VDD33_IO_2 (12)
VDD33_MAXBUS: VDD33_27 (M16), VDD33_28 (M18), VDD33_29 (M22)
VDD33_PCI (18): VDD33_30 (AC21), VDD33_31 (AD20), VDD33_32 (AD22), VDD33_33 (AH20), VDD33_34 (AH23), VDD33_35 (AH24), VDD33_36 (AH26), VDD33_37 (AH27), VDD33_38 (AL23), VDD33_39 (AL24), VDD33_40 (AL26), VDD33_41 (AL27), VDD33_42 (AL29), VDD33_43 (AL30), VDD33_44 (AP23), VDD33_45 (AP26), VDD33_46 (AP29), VDD33_47 (AP32)

=PP1V5_PWRON_I2_PLL

R2101 4.7 5% 1/16W MF-LF 402 — PP1V5_PWRON_I2_PLL1AVDD (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm)
R2102 4.7 5% 1/16W MF-LF 402 — PP1V5_PWRON_I2_PLL2AVDD (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm)
R2103 4.7 5% 1/16W MF-LF 402 — PP1V5_PWRON_I2_PLL3AVDD (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm)
R2104 4.7 5% 1/16W MF-LF 402 — PP1V5_PWRON_I2_PLL4AVDD (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm)
R2105 4.7 5% 1/16W MF-LF 402 — PP1V5_PWRON_I2_PLL5AVDD (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm)
R2106 4.7 5% 1/16W MF-LF 402 — PP1V5_PWRON_I2_PLL6AVDD (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm)
R2107 4.7 5% 1/16W MF-LF 402 — PP1V5_PWRON_I2_PLL7AVDD (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm)
R2109 4.7 5% 1/16W MF-LF 402 — PP1V5_PWRON_I2_PLL9AVDD (VOLTAGE=1.5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.2 mm)

C2101 C2102 C2103 C2104 C2105 C2106 C2107 C2109
1uF 10% 6.3V CERM 402

OMIT
U2100
I2
BGA
PLL POWER
(3 of 14)

PLL1 (AA20 PLL1_AVDD, Y20 PLL1_VSSA) 32/48 MHZ
PLL2 (AA19 PLL2_AVDD, Y19 PLL2_VSSA) 45.16 MHZ
PLL3 (AK19 PLL3_AVDD, AJ19 PLL3_VSSA) 49.15 MHZ
PLL4 (H9 PLL4_AVDD, H10 PLL4_VSSA) SYSCLK PCI(SS) AGP(SS)
PLL5 (AD9 PLL5_AVDD, AE9 PLL5_VSSA) INT REF PCI AGP ATA
PLL6 (M24 PLL6_AVDD, N24 PLL6_VSSA) SYS TRACK
PLL7 (AH22 PLL7_AVDD, AH21 PLL7_VSSA) PCI TRACK
PLL9 (AK10 PLL9_AVDD, AL10 PLL9_VSSA) AGP TRACK

OMIT
U2100
I2
BGA
CORE POWER & GND
(1 of 14)

VDD15_0 (AA22), VDD15_1 (AB21), VDD15_2 (AC16), VDD15_3 (AC19), VDD15_4 (N17), VDD15_5 (P16), VDD15_6 (P20), VDD15_7 (R16), VDD15_8 (R18), VDD15_9 (R21), VDD15_10 (T16), VDD15_11 (T19), VDD15_12 (T22), VDD15_13 (U16), VDD15_14 (U18), VDD15_15 (U20), VDD15_16 (U22), VDD15_17 (V17), VDD15_18 (V19), VDD15_19 (V22), VDD15_20 (W18), VDD15_21 (W20), VDD15_22 (W22), VDD15_23 (Y15), VDD15_24 (Y17)

VSS_0 (AA13), VSS_1 (AA15), VSS_2 (AA17), VSS_3 (AA21), VSS_4 (AA25), VSS_5 (AA29), VSS_6 (AB12), VSS_7 (AB15), VSS_8 (AB16), VSS_9 (AB22), VSS_10 (AB24), VSS_11 (AC2), VSS_12 (AC20), VSS_13 (AC25), VSS_14 (AC26), VSS_15 (AC29), VSS_16 (AC32), VSS_17 (AC35), VSS_18 (AC5), VSS_19 (AD16), VSS_20 (AD23), VSS_21 (AD29), VSS_22 (AE14), VSS_23 (AE15), VSS_24 (AE17), VSS_25 (AE19), VSS_26 (AE20), VSS_27 (AE25), VSS_28 (AF10), VSS_29 (AF18), VSS_30 (AF2), VSS_31 (AF27), VSS_32 (AF29), VSS_33 (AF32), VSS_34 (AF35), VSS_35 (AF5), VSS_36 (AF8), VSS_37 (AG11), VSS_38 (AG14), VSS_39 (AG29), VSS_40 (AH14), VSS_41 (AJ11), VSS_42 (AJ14), VSS_43 (AJ17), VSS_44 (AJ2), VSS_45 (AJ20), VSS_46 (AJ23), VSS_47 (AJ24), VSS_48 (AJ26), VSS_49 (AJ27)
VSS_50 (AJ29), VSS_51 (AJ32), VSS_52 (AJ35), VSS_53 (AJ5), VSS_54 (AJ8), VSS_55 (AM11), VSS_56 (AM14), VSS_57 (AM17), VSS_58 (AM2), VSS_59 (AM20), VSS_60 (AM23), VSS_61 (AM26), VSS_62 (AM29), VSS_63 (AM32), VSS_64 (AM35), VSS_65 (AM5), VSS_66 (AM7), VSS_67 (AM8), VSS_68 (AR11), VSS_69 (AR14), VSS_70 (AR17), VSS_71 (AR2), VSS_72 (AR20), VSS_73 (AR23), VSS_74 (AR26), VSS_75 (AR29), VSS_76 (AR32), VSS_77 (AR35), VSS_78 (AR5), VSS_79 (AR8), VSS_80 (B11), VSS_81 (B14), VSS_82 (B17), VSS_83 (B2), VSS_84 (B20), VSS_85 (B23), VSS_86 (B26), VSS_87 (B29), VSS_88 (B32), VSS_89 (B35), VSS_90 (B5), VSS_91 (B8), VSS_92 (E11), VSS_93 (E14), VSS_94 (E17), VSS_95 (E2), VSS_96 (E20), VSS_97 (E23), VSS_98 (E26), VSS_99 (E29)
VSS_100 (E32), VSS_101 (E35), VSS_102 (E5), VSS_103 (E8), VSS_104 (H11), VSS_105 (H12), VSS_106 (H14), VSS_107 (H15), VSS_108 (H17), VSS_109 (H18), VSS_110 (H2), VSS_111 (H20), VSS_112 (H23), VSS_113 (H24), VSS_114 (H26), VSS_115 (H27), VSS_116 (H29), VSS_117 (H32), VSS_118 (H35), VSS_119 (H5), VSS_120 (H8), VSS_121 (K10), VSS_122 (K11), VSS_123 (K14), VSS_124 (K17), VSS_125 (K20), VSS_126 (K23), VSS_127 (K25), VSS_128 (K26), VSS_129 (K29), VSS_130 (L2), VSS_131 (L20), VSS_132 (L27), VSS_133 (L29), VSS_134 (L32), VSS_135 (L35), VSS_136 (L5), VSS_137 (L8), VSS_138 (M13), VSS_139 (M15), VSS_140 (M17), VSS_141 (M19), VSS_142 (M21), VSS_143 (M23), VSS_144 (M26), VSS_145 (N14), VSS_146 (N16), VSS_147 (N18), VSS_148 (N23), VSS_149 (N25)
VSS_150 (P17), VSS_151 (P2), VSS_152 (P21), VSS_153 (P24), VSS_154 (P27), VSS_155 (P29), VSS_156 (P32), VSS_157 (P35), VSS_158 (P5), VSS_159 (P8), VSS_160 (R13), VSS_161 (R15), VSS_162 (R17), VSS_163 (R19), VSS_164 (R20), VSS_165 (R22), VSS_166 (R25), VSS_167 (R29), VSS_168 (T16), VSS_169 (T18), VSS_170 (T20), VSS_171 (U13), VSS_172 (U16), VSS_173 (U2), VSS_174 (U21), VSS_175 (U25), VSS_176 (U28), VSS_177 (U32), VSS_178 (U35), VSS_179 (U5), VSS_180 (U8), VSS_181 (V12), VSS_182 (V16), VSS_183 (V20), VSS_184 (V28), VSS_185 (W15), VSS_186 (W19), VSS_187 (W21), VSS_188 (W25), VSS_189 (W26), VSS_190 (Y11), VSS_191 (Y16), VSS_192 (Y18), VSS_193 (Y2), VSS_194 (Y22), VSS_195 (Y29), VSS_196 (Y32), VSS_197 (Y35), VSS_198 (Y5), VSS_199 (Y8)

I2 Power

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 21 OF 115	

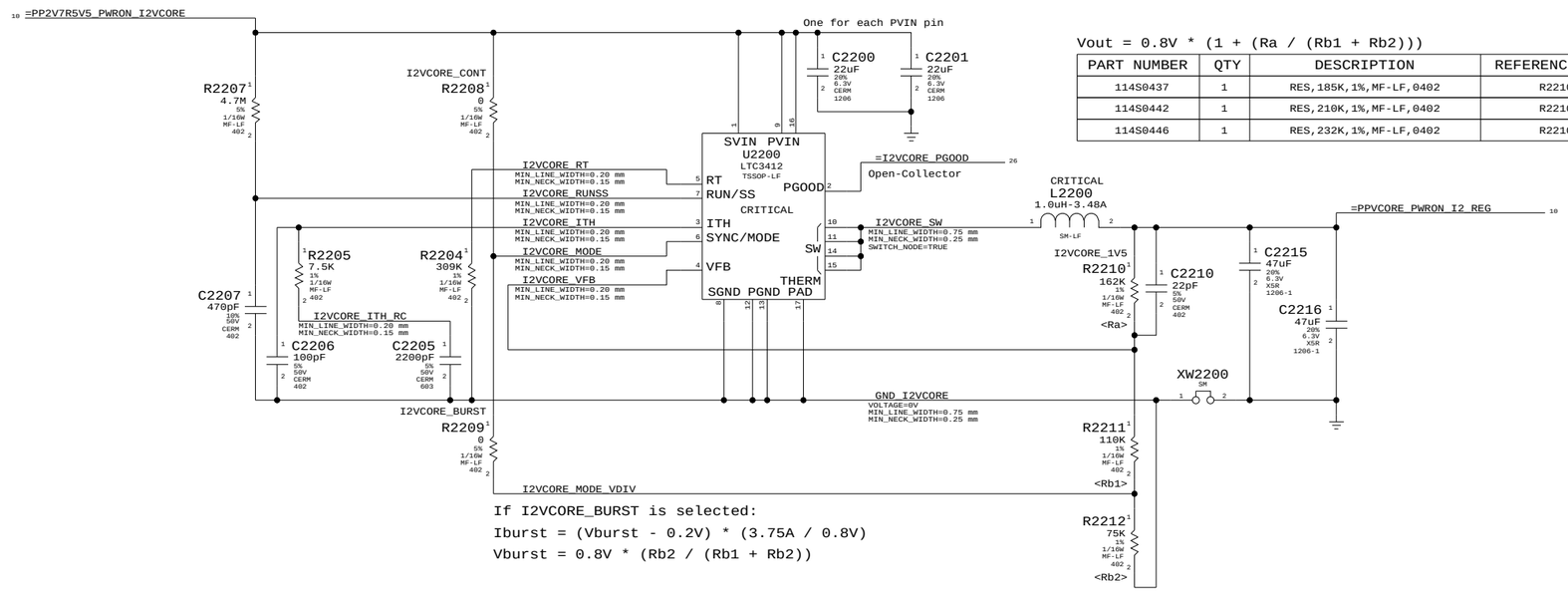
Page Notes

Power aliases required by this page:
- =PP2V7R5V5_PWRON_I2VCORE
- =PPVCORE_PWRON_I2_REG
- =PPVIN_PWRON_I2PLLVDD
- =PP1V5_PWRON_I2PLLVDD_LDO

Signal aliases required by this page:
- =I2VCORE_PGOOD

BOM options provided by this page:
- I2VCORE_CONT / I2VCORE_BURST
  Selects between forced continuous and burst mode for LTC3412 regulator.
- I2VCORE_xVx
  Selects appropriate resistor for the indicated LTC3412 output voltage.

I2 VCore Regulator



Vout = 0.8V * (1 + (Ra / (Rb1 + Rb2)))

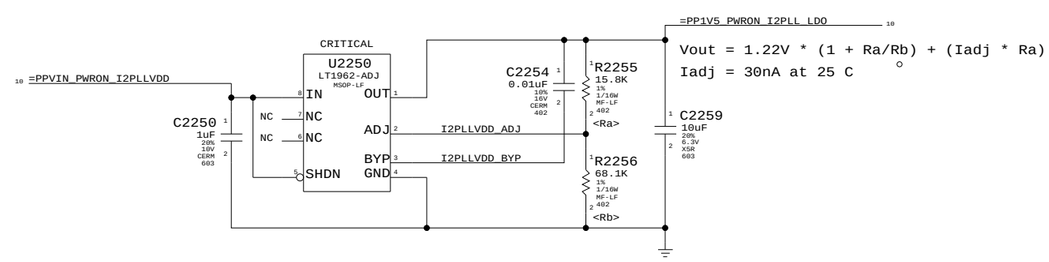
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0437	1	RES,185K,1%,MF-LF,0402	R2210		I2VCORE_1V6
114S0442	1	RES,210K,1%,MF-LF,0402	R2210		I2VCORE_1V7
114S0446	1	RES,232K,1%,MF-LF,0402	R2210		I2VCORE_1V8

If I2VCORE_BURST is selected:

Iburst = (Vburst - 0.2V) * (3.75A / 0.8V)

Vburst = 0.8V * (Rb2 / (Rb1 + Rb2))

I2 PLL LDO



Vout = 1.22V * (1 + Ra/Rb) + (Iadj * Ra)

Iadj = 30nA at 25 C

I2 Power Supplies

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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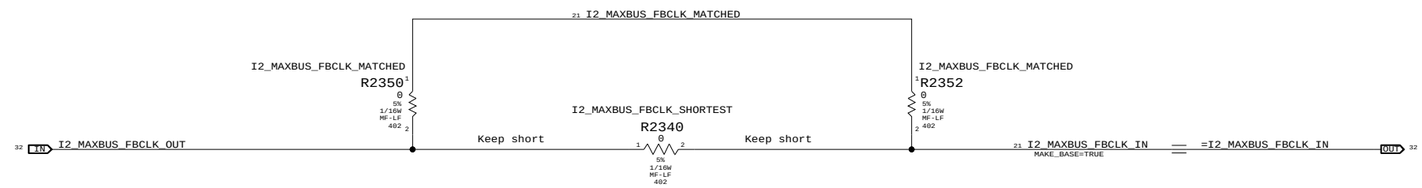
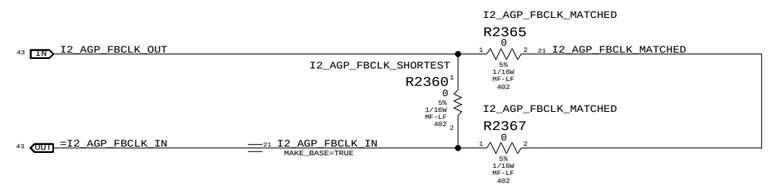
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 22 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_IN 21
	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_MATCHED 21
	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_IN 21
	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_MATCHED 21
1100	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_IN 21
1100	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_MATCHED 21
1110	CLOCK	CLOCK		=CLK33M_TBEN_SYNC 11 21
1120	CLOCK	CLOCK		=SYSCLK_TBEN_SYNC 11 21

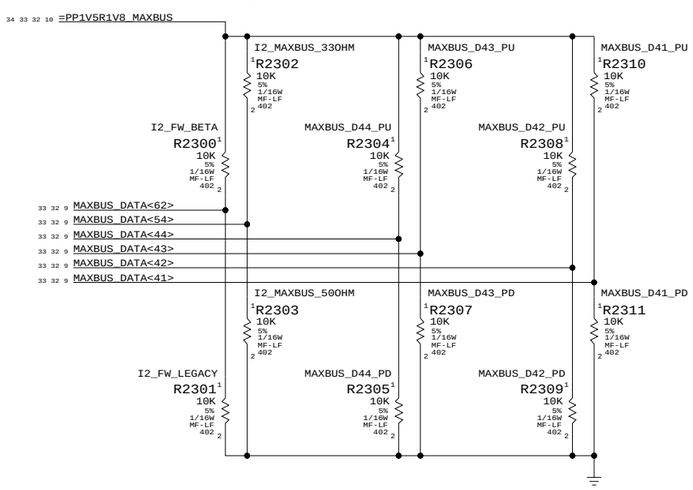
MaxBus Feedback Clock Network



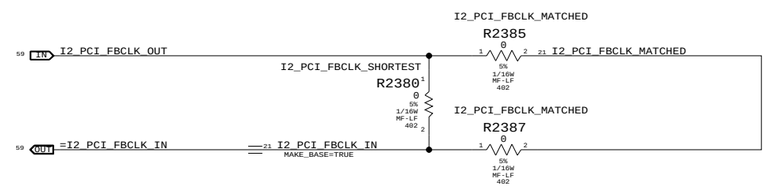
AGP Feedback Clock Ladder

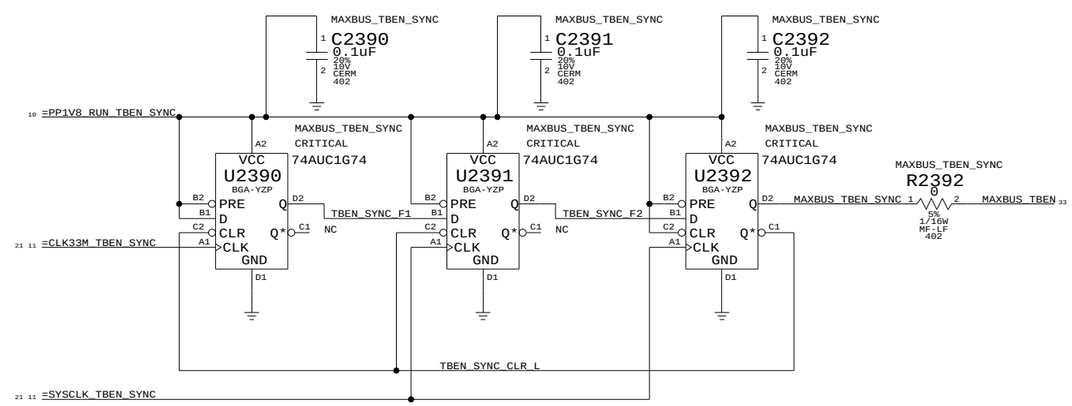


I2 Configuration Straps



PCI Feedback Clock Ladder





Signal	Tied	Description
MAXBUS_DATA<62>	HIGH	1394b Support (Beta Mode)
	LOW	1394a Support (Legacy Mode)
MAXBUS_DATA<54>	HIGH	50-Ohm MaxBus Drivers
	LOW	33-Ohm MaxBus Drivers
MAXBUS_DATA<44:41>	See Table Below	

BOM GROUP	Tied	Description	BOM OPTIONS
I2_MAXBUS_133MHZ	0000	133.12MHz CPU / 266.24MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_150MHZ	1000	149.76MHz CPU / 299.52MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_166MHZ	0100	166.40MHz CPU / 332.80MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_172MHZ	1100	171.95MHz CPU / 342.90MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_177MHZ	0010	177.49MHz CPU / 354.98MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_183MHZ	1010	183.04MHz CPU / 366.08MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_189MHZ	0110	188.59MHz CPU / 377.18MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_194MHZ	1110	194.13MHz CPU / 388.26MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_200MHZ	0001	199.68MHz CPU / 399.36MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PU

I2 Supplemental

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 23 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR
I2S0_DTI	I2S	I2S	
I2S0_DTO	I2S	I2S	
I2S0_MCLK	I2S	I2S	
I2S0_BITCLK	I2S	I2S	
I2S0_SYNC	I2S	I2S	
I2S1_DTI	I2S	I2S	
I2S1_DTO	I2S	I2S	
I2S1_MCLK	I2S	I2S	
I2S1_BITCLK	I2S	I2S	
I2S1_SYNC	I2S	I2S	
I2_XTAL	XTAL	XTAL	
(I2_XTAL)	XTAL	XTAL	
(I2_XTAL)	XTAL	XTAL	

I2S0_DEV_TO_SB_DTI 7 22 74
I2S0_SB_TO_DEV_DTO_R 6 22
I2S0_MCLK_R 6 22
I2S0_BITCLK_R 6 22
I2S0_SYNC_R 6 22
I2S1_DEV_TO_SB_DTI 22 30
I2S1_SB_TO_DEV_DTO_R 6 22
I2S1_MCLK_R 6 22
I2S1_BITCLK_R 6 22
I2S1_SYNC_R 6 22
I2_CLK18M_XOUT_R 22
I2_CLK18M_XOUT 22
I2_CLK18M_XIN 22

Page Notes

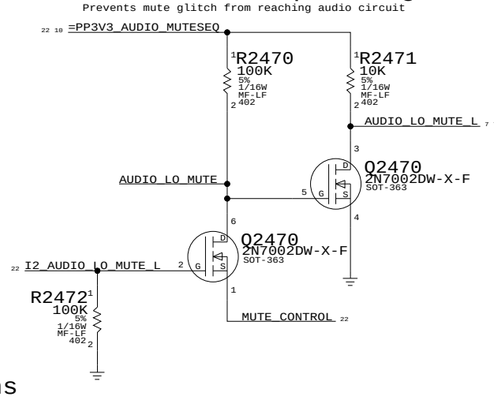
Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIOS (PWRON or PCI)
  Should be same as =PP3V3_PCI if slot E
  is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

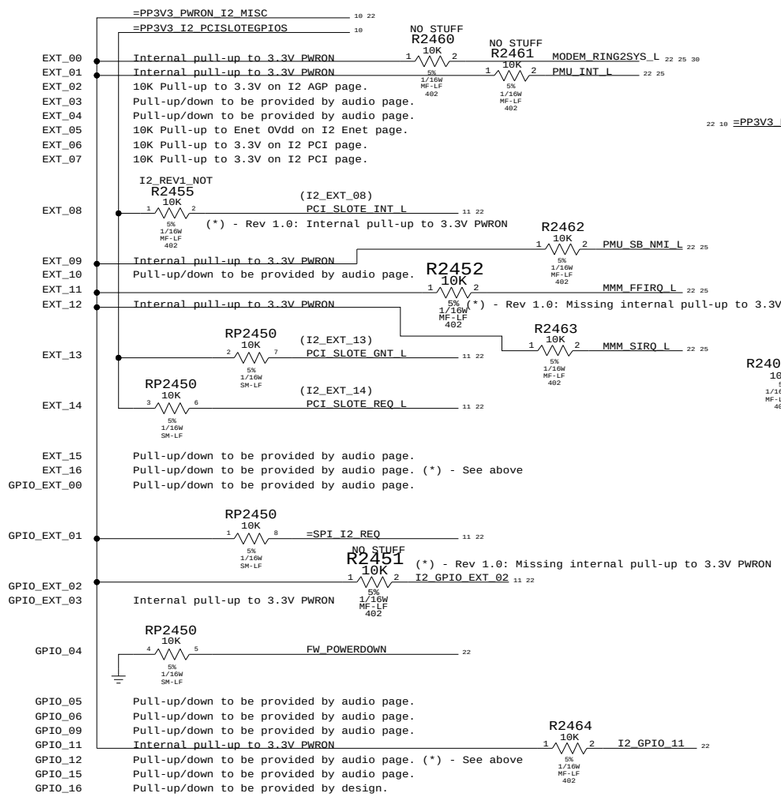
BOM options provided by this page:
- I2_REV1_NOT
  Use for I2 revisions > 1.0

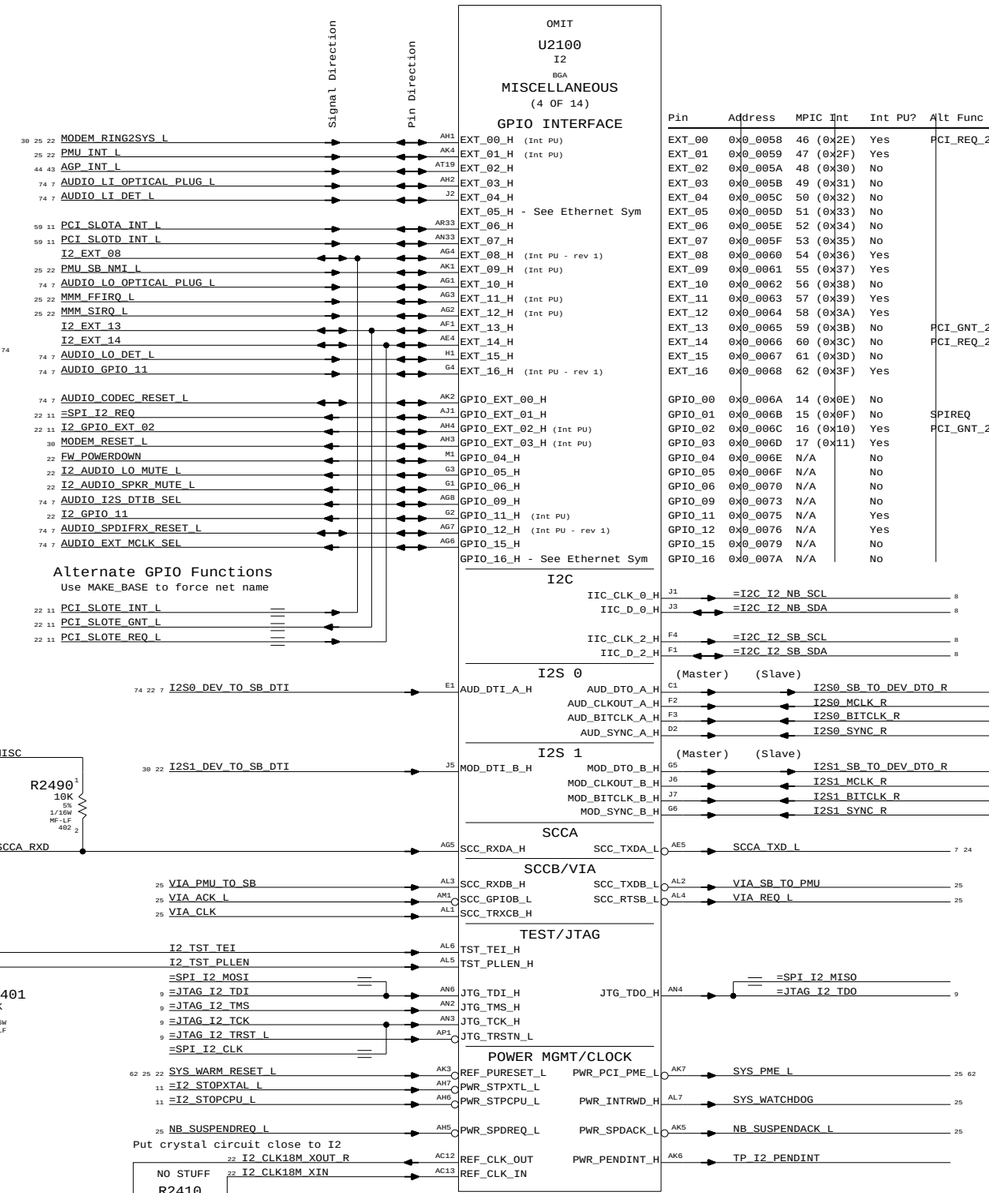
Audio Mute Sequencing

Prevents mute glitch from reaching audio circuit

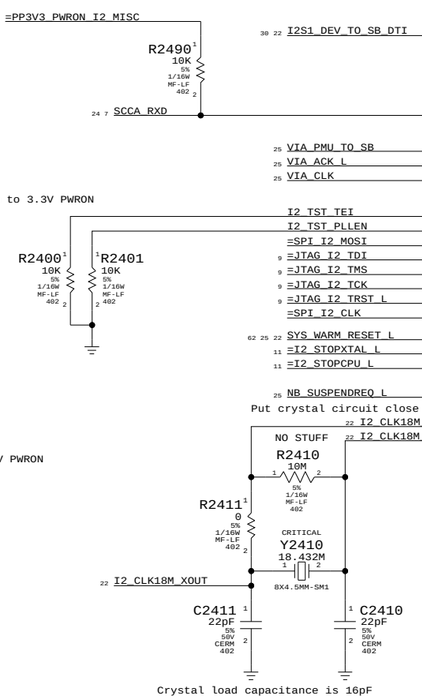


GPIO Pull-ups / Pull-downs



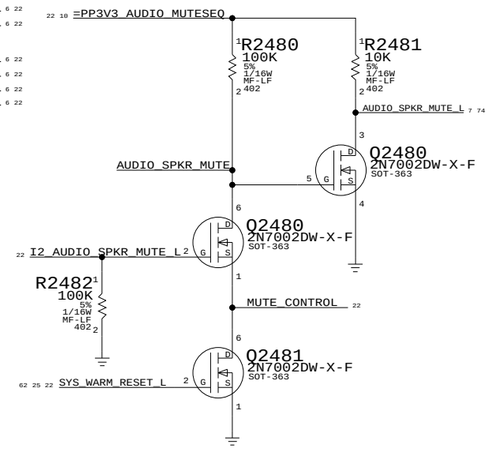


Pin	Address	MPIC Int	Int PU?	Alt Func
EXT_00	0x0_0058	46 (0x2E)	Yes	PCI_REQ_2_L (When PCI1_Slot2En = 10)
EXT_01	0x0_0059	47 (0x2F)	Yes	
EXT_02	0x0_005A	48 (0x30)	No	
EXT_03	0x0_005B	49 (0x31)	No	
EXT_04	0x0_005C	50 (0x32)	No	
EXT_05	0x0_005D	51 (0x33)	No	
EXT_06	0x0_005E	52 (0x34)	No	
EXT_07	0x0_005F	53 (0x35)	No	
EXT_08	0x0_0060	54 (0x36)	Yes	
EXT_09	0x0_0061	55 (0x37)	Yes	
EXT_10	0x0_0062	56 (0x38)	No	
EXT_11	0x0_0063	57 (0x39)	Yes	
EXT_12	0x0_0064	58 (0x3A)	Yes	
EXT_13	0x0_0065	59 (0x3B)	No	PCI_GNT_2_L (When PCI1_Slot2En = 11)
EXT_14	0x0_0066	60 (0x3C)	No	PCI_REQ_2_L (When PCI1_Slot2En = 11)
EXT_15	0x0_0067	61 (0x3D)	No	
EXT_16	0x0_0068	62 (0x3F)	Yes	
GPIO_00	0x0_006A	14 (0x0E)	No	
GPIO_01	0x0_006B	15 (0x0F)	No	SPIREQ (When SPISReqEn = 1)
GPIO_02	0x0_006C	16 (0x10)	Yes	PCI_GNT_2_L (When PCI1_Slot2En = 10)
GPIO_03	0x0_006D	17 (0x11)	Yes	
GPIO_04	0x0_006E	N/A	No	
GPIO_05	0x0_006F	N/A	No	
GPIO_06	0x0_0070	N/A	No	
GPIO_09	0x0_0073	N/A	No	
GPIO_11	0x0_0075	N/A	Yes	
GPIO_12	0x0_0076	N/A	Yes	
GPIO_15	0x0_0079	N/A	No	
GPIO_16	0x0_007A	N/A	No	



Audio Mute Sequencing

Prevents mute glitch from reaching audio circuit



I2 Miscellaneous

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 24 OF 115	

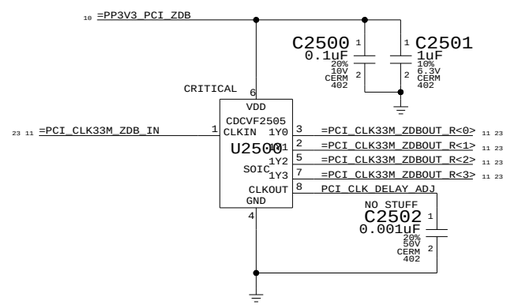
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
	CLOCK	CLOCK		=PCI_CLK33M_ZDB_IN 11 23
PCI_ZDBOUT0	CLOCK	CLOCK		=PCI_CLK33M_ZDBOUT_R<0> 11 23
PCI_ZDBOUT1	CLOCK	CLOCK		=PCI_CLK33M_ZDBOUT_R<1> 11 23
PCI_ZDBOUT2	CLOCK	CLOCK		=PCI_CLK33M_ZDBOUT_R<2> 11 23
PCI_ZDBOUT3	CLOCK	CLOCK		=PCI_CLK33M_ZDBOUT_R<3> 11 23

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIOS (PWRON or PCI)
  Should be same as =PP3V3_PCI if slot E
  is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- I2_REV1_NOT
  Use for I2 revisions > 1.0



PCI Clock Buffer

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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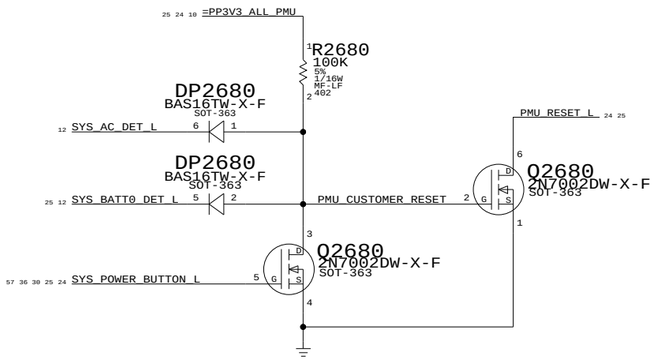
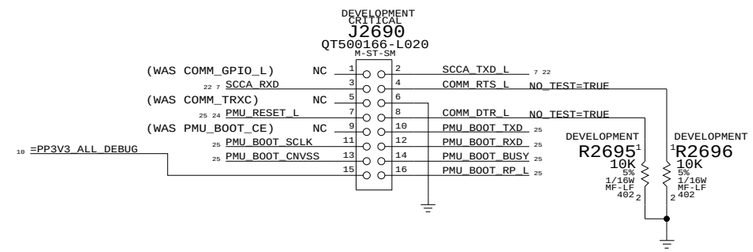
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 25 OF 115	

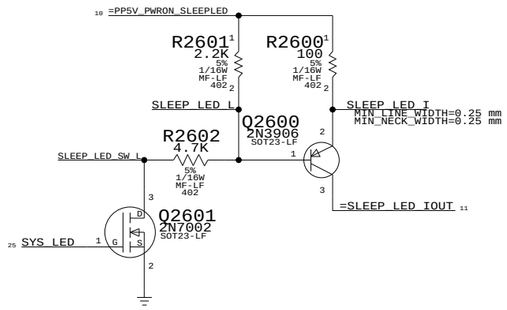
PMU RESET CIRCUIT



SERIAL DEBUG INTERFACE

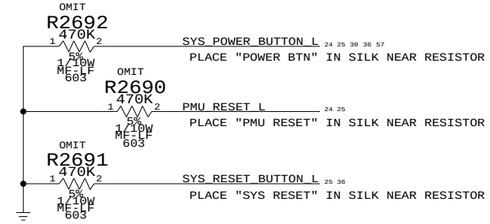


SLEEP LED

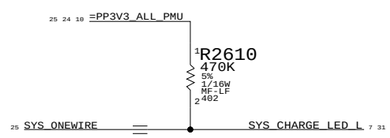


DEBUGGING AIDS

PLACE ON TOP SIDE NEAR FRONT EDGE OF BOARD



CHARGE LED



LEDs/Reset/Debug

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 26 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
PMU_CLK10M_XTAL	XTAL	XTAL		PMU_CLK10M_XIN 25
	XTAL	XTAL		PMU_CLK10M_XOUT 25
	XTAL	XTAL		PMU_CLK10M_XOUT_R 25
PMU_CLK32K_XTAL	XTAL	XTAL		PMU_CLK32K_XIN 25
	XTAL	XTAL		PMU_CLK32K_XOUT 25
	XTAL	XTAL		PMU_CLK32K_XOUT_R 25

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_PMU
- =PP3V3_PWRON_PMU
- =PPVREF_PMU (PMU AVCC or 2.5V reference)

Signal aliases required by this page:
- =I2C_PMU_SCL
- =I2C_PMU_SDA
- =I2C_PMU_SMB_SCL
- =I2C_PMU_SMB_SDA
- =JTAG_BBANGER_TCK
- =JTAG_BBANGER_TDI
- =JTAG_BBANGER_TMS
- =JTAG_BBANGER_TRST_L

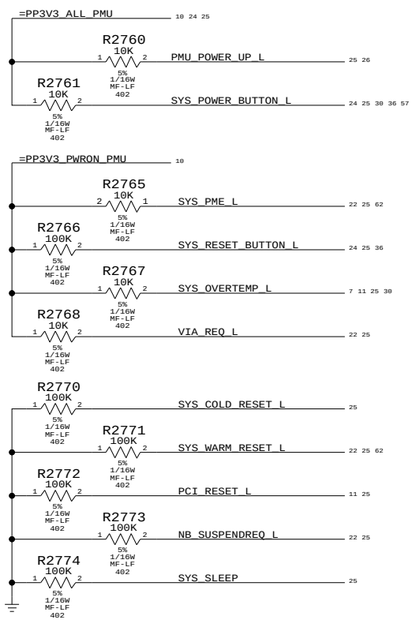
NOTE: Boot-banger pins can be aliased to TP_ or NC_ if not implemented.

BOM options provided by this page:
(NONE)

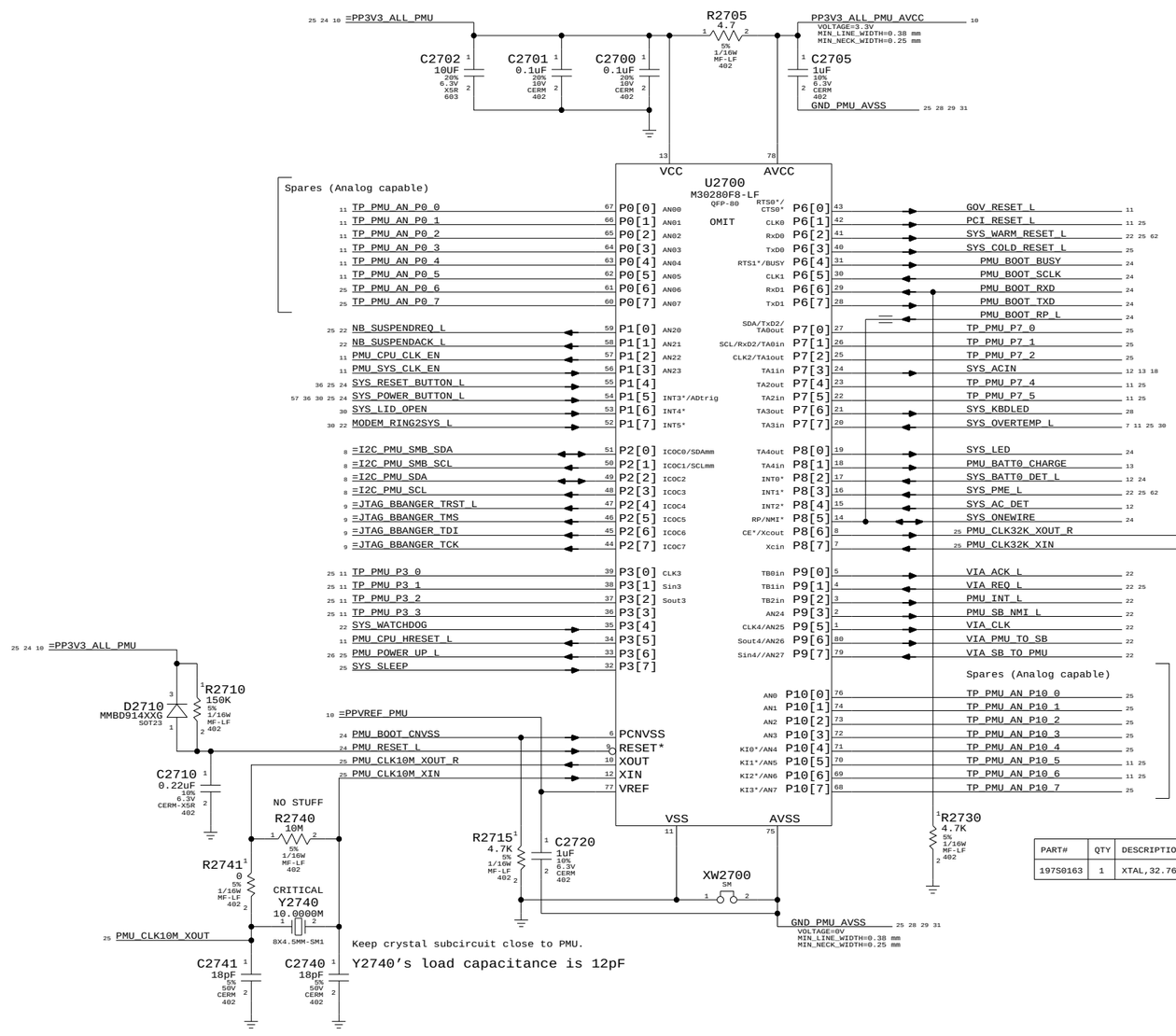
NOTE: TP_PMU_Px_x signals are general-purpose spares. Some pins are reserved for alternate functions. TP_PMU_AN_Px_x signals are general-purpose spares that can also be used as analog inputs.

NOTE: All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS signal (GND_PMU_AVSS). None of those capacitors are provided on this page.

PMU Pull-ups / pull-downs



Power Management Unit



Keep crystal subcircuit close to PMU.

Y2740's load capacitance is 12pF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0163	1	XTAL,32.768KHZ,4.1X1.5X0.9MM,SMD	Y2750	CRITICAL	?

Additional PMU05 "Modules"

MMM

25 TP_PMU_AN_P10_0	MMM_X_AXIS	29
25 TP_PMU_AN_P10_1	MMM_Y_AXIS	29
25 TP_PMU_AN_P10_2	MMM_Z_AXIS	29
25 TP_PMU_P7_0	MMM_FFIRQ_L	22
25 TP_PMU_P7_1	MMM_SIRQ_L	22
25 TP_PMU_AN_P0_7	MMM_ACC_SELFTEST	29
25 TP_PMU_AN_P0_6	MMM_ACC_PWRDOWN	29

ALS

25 TP_PMU_AN_P10_3	ALS_0_OUT	7 31
25 TP_PMU_AN_P10_4	ALS_1_OUT	28
25 TP_PMU_P7_2	ALS_GAIN_BOOST	7 28 31

CPU T-Diodes

25 11 TP_PMU_AN_P10_5	CPU0_TEMP	
25 11 TP_PMU_AN_P10_6	CPU1_TEMP	

SPI Dual Battery Charger

25 11 TP_PMU_P3_0	SPI_PMU_CHGR_CLK	
25 11 TP_PMU_P3_1	SPI_CHGR_TO_PMU_MISO	
25 11 TP_PMU_P3_2	SPI_PMU_TO_CHGR_MOSI	
25 11 TP_PMU_P3_3	SPI_PMU_CHGR_CS	
25 11 TP_PMU_P7_4	PMU_BATT1_DET_L	
25 11 TP_PMU_P7_5	PMU_BATT1_CHARGE	

Battery Current Mon

25 TP_PMU_AN_P10_7	BATT_ISNS	12

Power Management Unit (PMU05)

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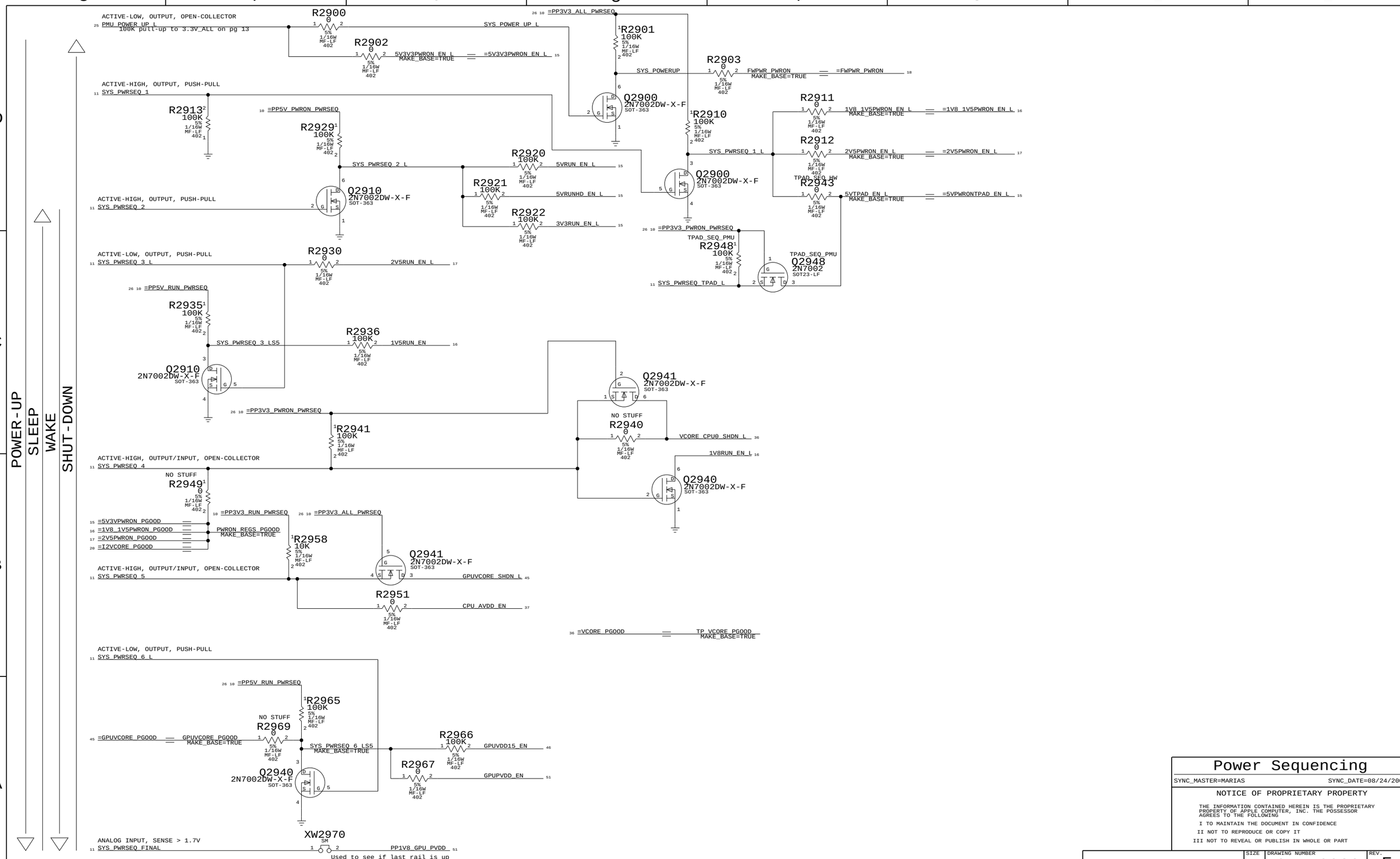

Power Sequencing

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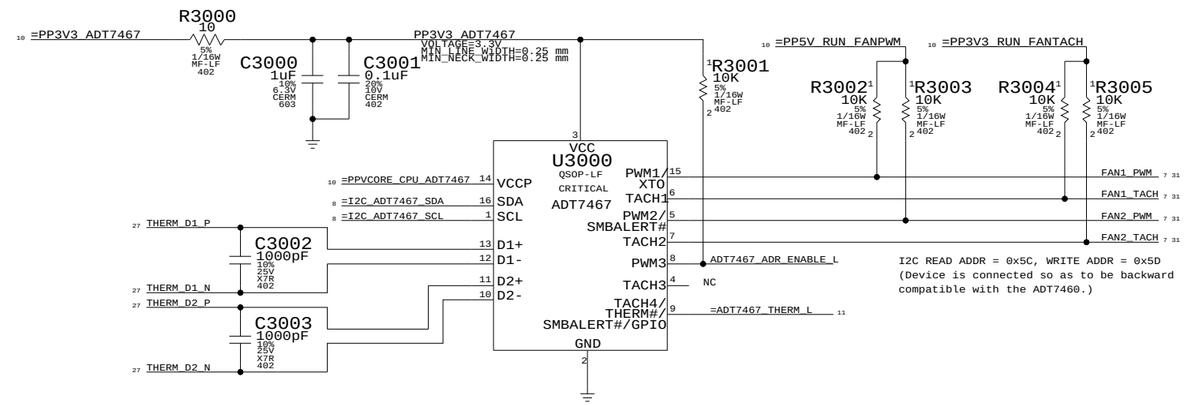
SCALE NONE	SHT 29 OF 115	

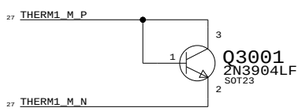
FAN CONTROLLER

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
1528	THERM	THERM	THERM1_M	THERM1_M_P
1529	THERM	THERM	THERM1_M	THERM1_M_N
1530	THERM	THERM	THERM2_M	THERM2_M_P
1531	THERM	THERM	THERM2_M	THERM2_M_N
1532	THERM	THERM	THERM1_A	THERM1_A_P
1533	THERM	THERM	THERM1_A	THERM1_A_N
1534	THERM	THERM	THERM2_A	THERM2_A_P
1535	THERM	THERM	THERM2_A	THERM2_A_N
1536	THERM	THERM	THERM_D1	THERM_D1_P
1537	THERM	THERM	THERM_D1	THERM_D1_N
1538	THERM	THERM	THERM_D2	THERM_D2_P
1539	THERM	THERM	THERM_D2	THERM_D2_N

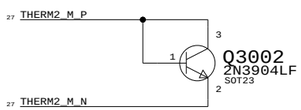


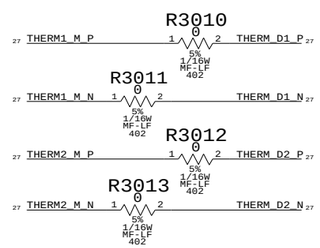
I2C READ ADDR = 0x5C, WRITE ADDR = 0x5D
(Device is connected so as to be backward compatible with the ADT7460.)

PLACE CLOSE TO CPU
MAIN1



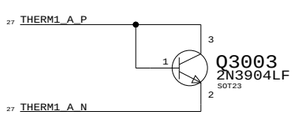
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



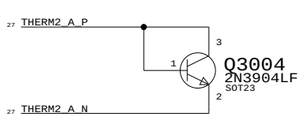


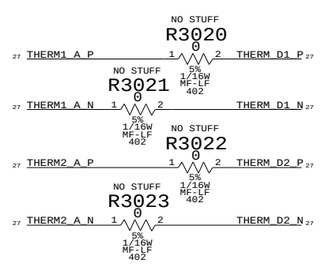
KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

PLACE UNDERNEATH UPPER RAM
ALTERNATE1



PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2





Fan Controller

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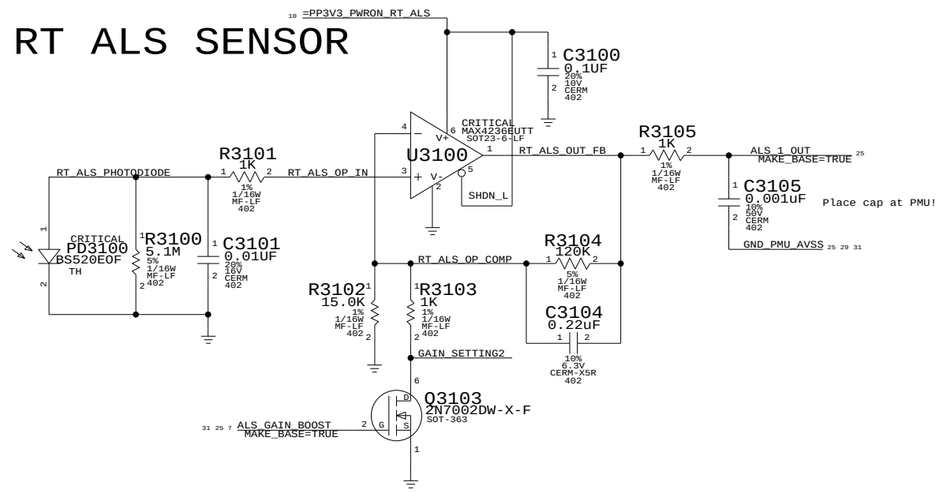
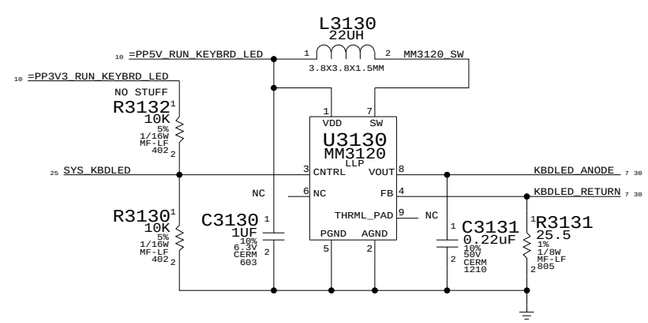
SCALE NONE	SHT 30 OF 115	

RT ALS SENSOR



PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1191	353S1186		U3100	Primary is unity gain stable/Alt is stable at G=5

Keyboard LED Driver



ALS Support

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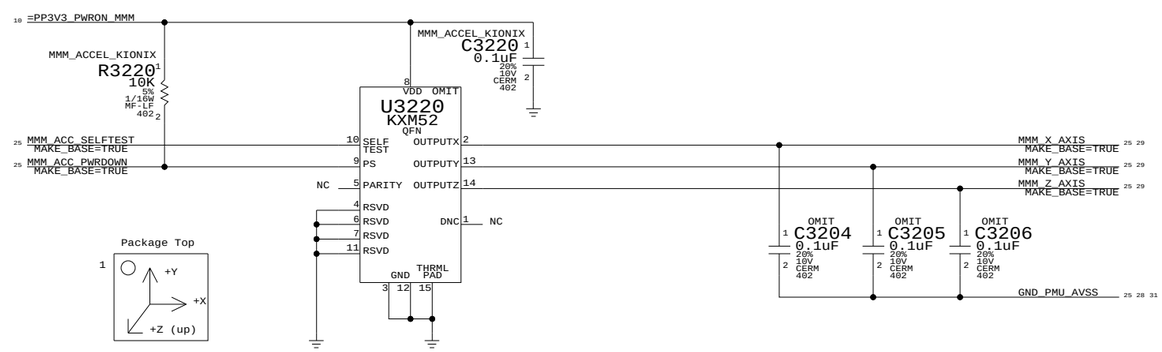
D	051-6839	E
SCALE NONE	SHT 31 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I67	THERM	THERM	
I68	THERM	THERM	
I69	THERM	THERM	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0222	1	IC,KIONIX,KXM52-2050,3AXIS ACCELEROMETER,SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0131	3	CAP,CER,0.033UF,10%,16V,X5R/X7R,0402,SMD	C3204,C3205,C3206	MMM_ACCEL_KIONIX

Sudden Motion Sensor

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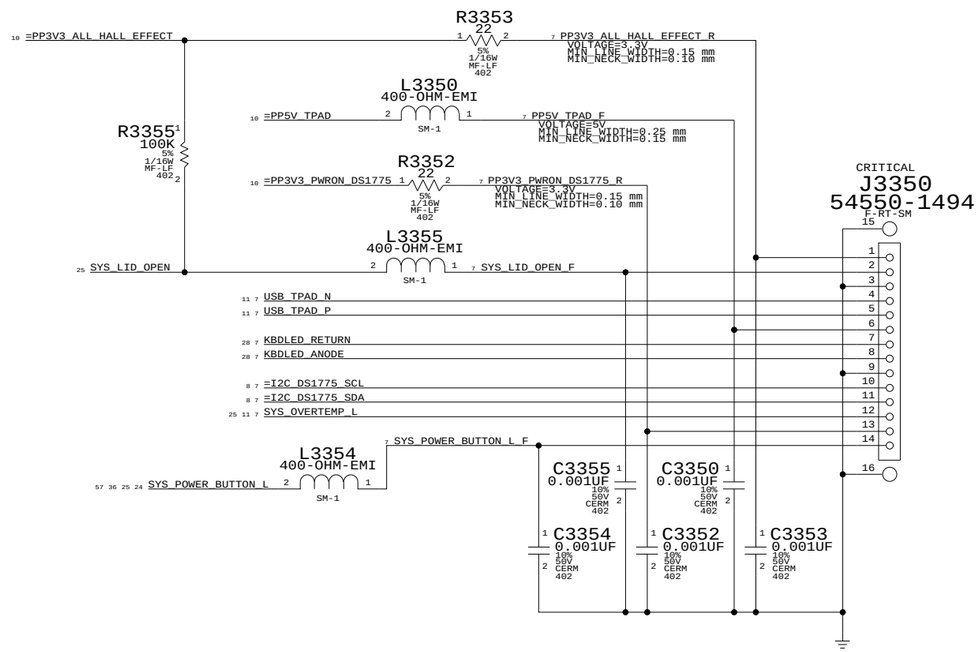
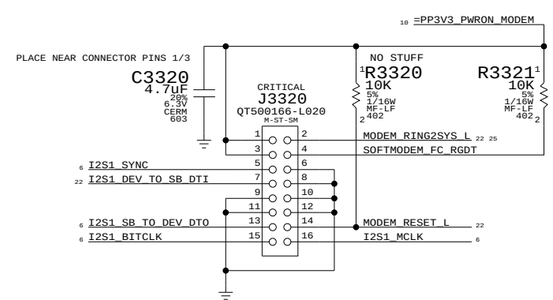
D	051-6839	E
SCALE NONE	SHT 32 OF 115	

USB Trackpad Conn



SOFT MODEM CONN



Q41C Internal I/O I	
SYNC_MASTER=N/A	SYNC_DATE=N/A

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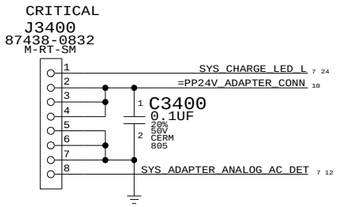
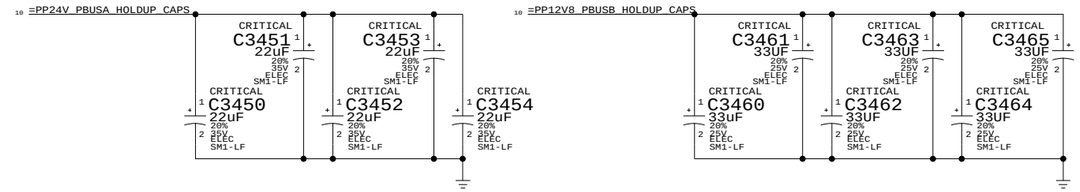
D	051-6839	E
SCALE NONE	SHT 33 OF 115	

ADAPTER CONNECTOR



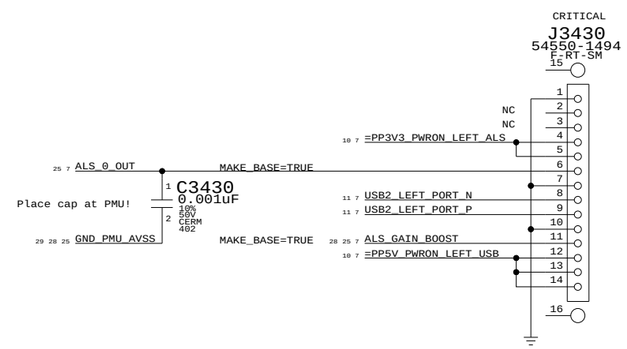
PBUS HOLD-UP CAPS



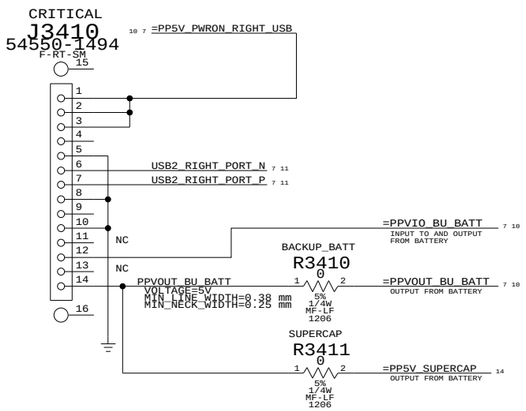
PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0085	126S0080		C3450,C3451,C3452,C3453,C3454	Primary is 260C/Alt is 250C part

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0084	126S0079		C3460,C3461,C3462,C3463,C3464,C3465	Primary is 260C/Alt is 250C part

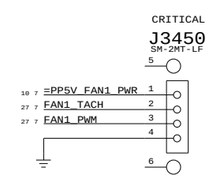
LEFT USB/LEFT ALS



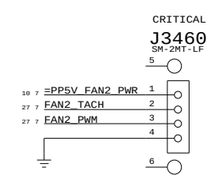
BACKUP BATTERY / RT USB CONNECTOR



CPU FAN



GPU FAN



Q41C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

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D	051-6839	E

SCALE NONE SHT 34 OF 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR
MAXBUS_CLK_CPU0	CLOCK	CLOCK	
MAXBUS_CLK_CPU1	CLOCK	CLOCK	
I2_MAXBUS_FBCLK	I2_FBCLK	I2_FBCLK	
	I2_FBCLK	I2_FBCLK	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_DATA41	MAXBUS	MAXBUS	
MAXBUS_DATA42	MAXBUS	MAXBUS	
MAXBUS_DATA43	MAXBUS	MAXBUS	
MAXBUS_DATA44	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_DATA54	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_DATA62	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPUS_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPUS_R	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR_R	MAXBUS	MAXBUS	
MAXBUS_CPUS_TO_NBIO	MAXBUS	MAXBUS	
MAXBUS_DTI	MAXBUS	MAXBUS	
MAXBUS_GBL_L	MAXBUS	MAXBUS	
MAXBUS_CPUS_TO_NBIO	MAXBUS	MAXBUS	
MAXBUS_CPUS_TO_NBIO	MAXBUS	MAXBUS	
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS	
MAXBUS_WT_L	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS	
MAXBUS_CPU0_TO_NB_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS	
MAXBUS_CPU0_DRDY_L	MAXBUS	MAXBUS	
MAXBUS_CPU0_TO_NB_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU1_R	MAXBUS	MAXBUS	
MAXBUS_CPU1_TO_NB_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU1_R	MAXBUS	MAXBUS	
MAXBUS_CPU1_DRDY_L	MAXBUS	MAXBUS	
MAXBUS_CPU1_TO_NB_R	MAXBUS	MAXBUS	

Page Notes

Power aliases required by this page:
- =PP1V5R1V8_RUN_I2_MAXBUS - =PP1V5R1V8_PWRON_I2_MAXBUS

BOM options provided by this page:
- MAXBUS_1V8 - Provides required voltage divider for FBCLK if MaxBus OVdd=1.8V.

Signal aliases required by this page:
- =I2_MAXBUS_FBCLK_IN - MaxBus feedback clock input. Length should match that of clock(s) from I2 to CPU(s).

MaxBus I/O DECOUPLING

(41 Balls on I2)

OMIT
U2100
I2
BGA
MAXBUS POWER
(6 of 14)

VDD18_0 C11, VDD18_1 C14, VDD18_2 C17, VDD18_3 C20, VDD18_4 C23, VDD18_5 C26, VDD18_6 C29, VDD18_7 C3, VDD18_8 C32, VDD18_9 C8, VDD18_10 F11, VDD18_11 F14, VDD18_12 F17, VDD18_13 F20, VDD18_14 F23, VDD18_15 F26, VDD18_16 F29, VDD18_17 F8, VDD18_18 J11, VDD18_19 J12, VDD18_20 J14, VDD18_21 J15, VDD18_22 J17, VDD18_23 J18, VDD18_24 J20, VDD18_25 J23, VDD18_26 J24, VDD18_27 J26, VDD18_28 J27, VDD18_29 L14, VDD18_30 L17, VDD18_31 L23, VDD18_32 M20, VDD18_33 N15, VDD18_34 N19, VDD18_35 N21, VDD18_36 N22, VDD18_37 P14, VDD18_38 P15, VDD18_39 P18, VDD18_40 P22

PP1V5R1V8_I2_MAXBUS
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

1 X 10uF (0603)
41 X 1uF (0402)

C3550 C3551 C3552 C3553 C3554 C3555 C3556 C3557 C3558 C3559 C3560 C3561 C3562 C3563 C3564 C3565 C3566 C3567 C3568 C3569 C3570 C3571 C3572 C3573 C3574 C3575 C3576 C3577 C3578 C3579 C3580 C3581 C3582 C3583 C3584 C3585 C3586 C3587 C3588 C3589 C3590
1uF 10% 6.3V CERM 402

C3599 10uF 20% 6.3V X5R 603

R3550 0 5% 1/10W MF-LF 603 =PP1V5R1V8_RUN_I2_MAXBUS 10

NO STUFF
R3551 0 5% 1/10W MF-LF 603 =PP1V5R1V8_PWRON_I2_MAXBUS 10

OMIT
U2100
I2
BGA
PROCESSOR INTERFACE
(5 of 14)

PROCESSOR 0

33 32 MAXBUS_CPU0_QREQ_L	E25	MAX_QREQ_0_L	MAX_QACK_0_L	F18	MAXBUS_CPU0_QACK_L 33
33 32 6 MAXBUS_CPU0_BR_L	F21	MAX_BR_0_L	MAX_BG_0_L	E22	MAXBUS_CPU0_BG_L 6 32 33
33 32 6 MAXBUS_CPU0_DRDY_L	G25	MAX_DRDY_0_L	MAX_DBG_0_L	F24	MAXBUS_CPU0_DBG_L 6 32 33
33 32 6 MAXBUS_CPU0_HIT_L	E21	MAX_HIT_0_L	CPU_INT_0_L	J19	MAXBUS_CPU0_INT_L 6 34
			MAX_CLK_0_H	H21	MAXBUS_CLK_CPU0_R 11 32

PROCESSOR 1

32 MAXBUS_CPU1_QREQ_L	E27	MAX_QREQ_1_L	MAX_QACK_1_L	G18	TP_MAXBUS_CPU1_QACK_L 11
32 6 MAXBUS_CPU1_BR_L	G21	MAX_BR_1_L	MAX_BG_1_L	E24	MAXBUS_CPU1_BG_L 6 32
32 6 MAXBUS_CPU1_DRDY_L	F25	MAX_DRDY_1_L	MAX_DBG_1_L	G24	MAXBUS_CPU1_DBG_L 6 32
32 6 MAXBUS_CPU1_HIT_L	C21	MAX_HIT_1_L	CPU_INT_1_L	H19	MAXBUS_CPU1_INT_L 6
			MAX_CLK_1_H	J21	TP_MAXBUS_CLK_CPU1_R 11 32

MAXBUS INTERFACE

33 32 6 MAXBUS_TS_L	B27	MAX_TS_L	MAX_AACK_L	A31	MAXBUS_AACK_L 6 32 33
33 32 6 MAXBUS_ARTRY_L	C30	MAX_ARTRY_L			
33 32 9 MAXBUS_ADDR<0>	D18	MAX_A_00_H	MAX_D_00_H	D16	MAXBUS_DATA<0> 9 32 33
33 32 9 MAXBUS_ADDR<1>	A28	MAX_A_01_H	MAX_D_01_H	A10	MAXBUS_DATA<1> 9 32 33
33 32 9 MAXBUS_ADDR<2>	A19	MAX_A_02_H	MAX_D_02_H	A9	MAXBUS_DATA<2> 9 32 33
33 32 9 MAXBUS_ADDR<3>	A23	MAX_A_03_H	MAX_D_03_H	D12	MAXBUS_DATA<3> 9 32 33
33 32 9 MAXBUS_ADDR<4>	D21	MAX_A_04_H	MAX_D_04_H	A11	MAXBUS_DATA<4> 9 32 33
33 32 9 MAXBUS_ADDR<5>	A25	MAX_A_05_H	MAX_D_05_H	B10	MAXBUS_DATA<5> 9 32 33
33 32 9 MAXBUS_ADDR<6>	A18	MAX_A_06_H	MAX_D_06_H	C10	MAXBUS_DATA<6> 9 32 33
33 32 9 MAXBUS_ADDR<7>	C28	MAX_A_07_H	MAX_D_07_H	G16	MAXBUS_DATA<7> 9 32 33
33 32 9 MAXBUS_ADDR<8>	D25	MAX_A_08_H	MAX_D_08_H	D9	MAXBUS_DATA<8> 9 32 33
33 32 9 MAXBUS_ADDR<9>	B31	MAX_A_09_H	MAX_D_09_H	C9	MAXBUS_DATA<9> 9 32 33
33 32 9 MAXBUS_ADDR<10>	B24	MAX_A_10_H	MAX_D_10_H	F15	MAXBUS_DATA<10> 9 32 33
33 32 9 MAXBUS_ADDR<11>	G28	MAX_A_11_H	MAX_D_11_H	G15	MAXBUS_DATA<11> 9 32 33
33 32 9 MAXBUS_ADDR<12>	C25	MAX_A_12_H	MAX_D_12_H	B9	MAXBUS_DATA<12> 9 32 33
33 32 9 MAXBUS_ADDR<13>	D31	MAX_A_13_H	MAX_D_13_H	D10	MAXBUS_DATA<13> 9 32 33
33 32 9 MAXBUS_ADDR<14>	F19	MAX_A_14_H	MAX_D_14_H	E15	MAXBUS_DATA<14> 9 32 33
33 32 9 MAXBUS_ADDR<15>	E30	MAX_A_15_H	MAX_D_15_H	C7	MAXBUS_DATA<15> 9 32 33
33 32 9 MAXBUS_ADDR<16>	D27	MAX_A_16_H	MAX_D_16_H	B7	MAXBUS_DATA<16> 9 32 33
33 32 9 MAXBUS_ADDR<17>	A27	MAX_A_17_H	MAX_D_17_H	A8	MAXBUS_DATA<17> 9 32 33
33 32 9 MAXBUS_ADDR<18>	B28	MAX_A_18_H	MAX_D_18_H	F16	MAXBUS_DATA<18> 9 32 33
33 32 9 MAXBUS_ADDR<19>	B25	MAX_A_19_H	MAX_D_19_H	G13	MAXBUS_DATA<19> 9 32 33
33 32 9 MAXBUS_ADDR<20>	E19	MAX_A_20_H	MAX_D_20_H	E13	MAXBUS_DATA<20> 9 32 33
33 32 9 MAXBUS_ADDR<21>	G27	MAX_A_21_H	MAX_D_21_H	E12	MAXBUS_DATA<21> 9 32 33
33 32 9 MAXBUS_ADDR<22>	D30	MAX_A_22_H	MAX_D_22_H	D7	MAXBUS_DATA<22> 9 32 33
33 32 9 MAXBUS_ADDR<23>	C31	MAX_A_23_H	MAX_D_23_H	A7	MAXBUS_DATA<23> 9 32 33
33 32 9 MAXBUS_ADDR<24>	F28	MAX_A_24_H	MAX_D_24_H	G12	MAXBUS_DATA<24> 9 32 33
33 32 9 MAXBUS_ADDR<25>	F27	MAX_A_25_H	MAX_D_25_H	F12	MAXBUS_DATA<25> 9 32 33
33 32 9 MAXBUS_ADDR<26>	B30	MAX_A_26_H	MAX_D_26_H	F13	MAXBUS_DATA<26> 9 32 33
33 32 9 MAXBUS_ADDR<27>	E28	MAX_A_27_H	MAX_D_27_H	A6	MAXBUS_DATA<27> 9 32 33
33 32 9 MAXBUS_ADDR<28>	B18	MAX_A_28_H	MAX_D_28_H	E10	MAXBUS_DATA<28> 9 32 33
33 32 9 MAXBUS_ADDR<29>	C22	MAX_A_29_H	MAX_D_29_H	B6	MAXBUS_DATA<29> 9 32 33
33 32 9 MAXBUS_ADDR<30>	A17	MAX_A_30_H	MAX_D_30_H	C6	MAXBUS_DATA<30> 9 32 33
33 32 9 MAXBUS_ADDR<31>	B19	MAX_A_31_H	MAX_D_31_H	D6	MAXBUS_DATA<31> 9 32 33
			MAX_D_32_H	G7	MAXBUS_DATA<32> 9 32 33
			MAX_D_33_H	A3	MAXBUS_DATA<33> 9 32 33
33 32 9 MAXBUS_CI_L	A26	MAX_CI_L	MAX_D_34_H	E6	MAXBUS_DATA<34> 9 32 33
33 32 9 MAXBUS_GBL_L	A24	MAX_GBL_L	MAX_D_35_H	F7	MAXBUS_DATA<35> 9 32 33
33 32 9 MAXBUS_TBST_L	E16	MAX_TBST_L	MAX_D_36_H	C4	MAXBUS_DATA<36> 9 32 33
33 32 9 MAXBUS_TSIZ<0>	D19	MAX_TSIZ_0_H	MAX_D_37_H	D3	MAXBUS_DATA<37> 9 32 33
33 32 9 MAXBUS_TSIZ<1>	C18	MAX_TSIZ_1_H	MAX_D_38_H	G9	MAXBUS_DATA<38> 9 32 33
33 32 9 MAXBUS_TSIZ<2>	B21	MAX_TSIZ_2_H	MAX_D_39_H	D4	MAXBUS_DATA<39> 9 32 33
33 32 9 MAXBUS_TT<0>	B22	MAX_TT_0_H	MAX_D_40_H	B16	MAXBUS_DATA<40> 9 32 33
33 32 9 MAXBUS_TT<1>	D22	MAX_TT_1_H	MAX_D_41_H	C16	MAXBUS_DATA<41> 9 21 32 33
33 32 9 MAXBUS_TT<2>	E18	MAX_TT_2_H	MAX_D_42_H	A13	MAXBUS_DATA<42> 9 21 32 33
33 32 9 MAXBUS_TT<3>	A21	MAX_TT_3_H	MAX_D_43_H	A16	MAXBUS_DATA<43> 9 21 32 33
33 32 9 MAXBUS_TT<4>	A22	MAX_TT_4_H	MAX_D_44_H	C13	MAXBUS_DATA<44> 9 21 32 33
33 32 9 MAXBUS_WT_L	D24	MAX_WT_L	MAX_D_45_H	B15	MAXBUS_DATA<45> 9 32 33
			MAX_D_46_H	D15	MAXBUS_DATA<46> 9 32 33
			MAX_D_47_H	B12	MAXBUS_DATA<47> 9 32 33
			MAX_D_48_H	A14	MAXBUS_DATA<48> 9 32 33
			MAX_D_49_H	A12	MAXBUS_DATA<49> 9 32 33
			MAX_D_50_H	D13	MAXBUS_DATA<50> 9 32 33
			MAX_D_51_H	B13	MAXBUS_DATA<51> 9 32 33
			MAX_D_52_H	A15	MAXBUS_DATA<52> 9 32 33
			MAX_D_53_H	C15	MAXBUS_DATA<53> 9 32 33
			MAX_D_54_H	C5	MAXBUS_DATA<54> 9 21 32 33
			MAX_D_55_H	C12	MAXBUS_DATA<55> 9 32 33
			MAX_D_56_H	F6	MAXBUS_DATA<56> 9 32 33
			MAX_D_57_H	A5	MAXBUS_DATA<57> 9 32 33
			MAX_D_58_H	F9	MAXBUS_DATA<58> 9 32 33
			MAX_D_59_H	E9	MAXBUS_DATA<59> 9 32 33
			MAX_D_60_H	E7	MAXBUS_DATA<60> 9 32 33
			MAX_D_61_H	G10	MAXBUS_DATA<61> 9 32 33
			MAX_D_62_H	B4	MAXBUS_DATA<62> 9 21 32 33
			MAX_D_63_H	F10	MAXBUS_DATA<63> 9 32 33
			MAX_DTI_0_H	C27	MAXBUS_DTI<0> 9 32 33
			MAX_DTI_1_H	A30	MAXBUS_DTI<1> 9 32 33
			MAX_DTI_2_H	A29	MAXBUS_DTI<2> 9 32 33
			MAX_TA_L	G19	MAXBUS_TA_L 6 32 33
			MAX_TEA_L	D28	MAXBUS_TEA_L 6 32 33
			MAX_TBEN_H	C24	TP_MAXBUS_TBEN_I2
			MAX_FBCLK_OUT_H	J22	32 I2_MAXBUS_FBCLK_OUT_R

I2_ACS_REF — K9 ACS_REF_H

R3500 1K 1% 1/16W MF-LF 402

21 =I2_MAXBUS_FBCLK_IN

MAXBUS_1V8
R3506 360 5% 1/16W MF-LF 402

1.5V IN

1.5V-1.8V OUT (Matches MaxBus OVdd)
Output impedance is 50 Ohms

R3505 10 5% 1/16W MF-LF 402 — I2_MAXBUS_FBCLK_OUT — 21 32

MaxBus Pull-ups / Pull-downs

34 33 21 10 =PP1V5R1V8_MAXBUS

One resistor for each of:
- MAXBUS_TS_L
- MAXBUS_TA_L
- MAXBUS_TEA_L
- MAXBUS_ARTRY_L
- MAXBUS_AACK_L
- (Spare)

6 =RP3510P1 — RP3510 10K 5% 1/16W SM-LF
6 =RP3510P2 — RP3510 10K 5% 1/16W SM-LF
6 =RP3510P3 — RP3510 10K 5% 1/16W SM-LF
6 =RP3510P4 — RP3510 10K 5% 1/16W SM-LF
6 =RP3511P1 — RP3511 10K 5% 1/16W SM-LF
6 =RP3511P2 — RP3511 10K 5% 1/16W SM-LF

I2 CPU0 Support

One resistor for each of:
- MAXBUS_CPU0_BR_L
- MAXBUS_CPU0_BG_L
- MAXBUS_CPU0_DBG_L
- MAXBUS_CPU0_DRDY_L
- MAXBUS_CPU0_HIT_L
- MAXBUS_CPU0_INT_L

6 =RP3511P3 — RP3511 10K 5% 1/16W SM-LF
6 =RP3511P4 — RP3511 10K 5% 1/16W SM-LF
6 =RP3512P1 — RP3512 10K 5% 1/16W SM-LF
6 =RP3512P2 — RP3512 10K 5% 1/16W SM-LF
6 =RP3512P3 — RP3512 10K 5% 1/16W SM-LF
6 =RP3512P4 — RP3512 10K 5% 1/16W SM-LF
33 32 MAXBUS_CPU0_QREQ_L — R3513 10K 5% 1/16W MF-LF 402

I2 CPU1 Support

One resistor for each of:
- MAXBUS_CPU1_BR_L
- MAXBUS_CPU1_BG_L
- MAXBUS_CPU1_DBG_L
- MAXBUS_CPU1_DRDY_L
- MAXBUS_CPU1_HIT_L
- MAXBUS_CPU1_INT_L

6 =RP3513P2 — RP3513 10K 5% 1/16W SM-LF
6 =RP3513P3 — RP3513 10K 5% 1/16W SM-LF
6 =RP3513P4 — RP3513 10K 5% 1/16W SM-LF
6 =RP3514P1 — RP3514 10K 5% 1/16W SM-LF
6 =RP3514P2 — RP3514 10K 5% 1/16W SM-LF
6 =RP3514P3 — RP3514 10K 5% 1/16W SM-LF
32 MAXBUS_CPU1_QREQ_L — R3514 10K 5% 1/16W MF-LF 402

I2 Processor Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 35 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PBUS	CLOCK	CLOCK	

=MAXBUS_CPU0_CLK 11 33

Page Notes

Power aliases required by this page:
- =PP1V5R1V8_MAXBUS

Signal aliases required by this page:
- =MAXBUS_CPU0_CLK

BOM options provided by this page:
(NONE)

U3600 (2 OF 6)

BGA, XXGHZ-XXV, A0-X.X, OMIT, CRITICAL

Signal	Pin	Signal	Pin
_MAXBUS_DATA<0>	R15	D0	
_MAXBUS_DATA<1>	W15	D1	
_MAXBUS_DATA<2>	T14	D2	
_MAXBUS_DATA<3>	V16	D3	
_MAXBUS_DATA<4>	W16	D4	
_MAXBUS_DATA<5>	T15	D5	
_MAXBUS_DATA<6>	U15	D6	
_MAXBUS_DATA<7>	P14	D7	
_MAXBUS_DATA<8>	V13	D8	
_MAXBUS_DATA<9>	W13	D9	
_MAXBUS_DATA<10>	T13	D10	
_MAXBUS_DATA<11>	P13	D11	
_MAXBUS_DATA<12>	U14	D12	
_MAXBUS_DATA<13>	W14	D13	
_MAXBUS_DATA<14>	R12	D14	
_MAXBUS_DATA<15>	T12	D15	
_MAXBUS_DATA<16>	W12	D16	
_MAXBUS_DATA<17>	V12	D17	
_MAXBUS_DATA<18>	N11	D18	
_MAXBUS_DATA<19>	N10	D19	
_MAXBUS_DATA<20>	R11	D20	
_MAXBUS_DATA<21>	U11	D21	
_MAXBUS_DATA<22>	W11	D22	
_MAXBUS_DATA<23>	T11	D23	
_MAXBUS_DATA<24>	R10	D24	
_MAXBUS_DATA<25>	N9	D25	
_MAXBUS_DATA<26>	P10	D26	
_MAXBUS_DATA<27>	U10	D27	
_MAXBUS_DATA<28>	R9	D28	
_MAXBUS_DATA<29>	W10	D29	
_MAXBUS_DATA<30>	U9	D30	
_MAXBUS_DATA<31>	V9	D31	
_MAXBUS_DATA<32>	W5	D32	
_MAXBUS_DATA<33>	U6	D33	
_MAXBUS_DATA<34>	T5	D34	
_MAXBUS_DATA<35>	U5	D35	
_MAXBUS_DATA<36>	W7	D36	
_MAXBUS_DATA<37>	R6	D37	
_MAXBUS_DATA<38>	P7	D38	
_MAXBUS_DATA<39>	V6	D39	
_MAXBUS_DATA<40>	P17	D40	
_MAXBUS_DATA<41>	R19	D41	
_MAXBUS_DATA<42>	V18	D42	
_MAXBUS_DATA<43>	R18	D43	
_MAXBUS_DATA<44>	V19	D44	
_MAXBUS_DATA<45>	T19	D45	
_MAXBUS_DATA<46>	U19	D46	
_MAXBUS_DATA<47>	W19	D47	
_MAXBUS_DATA<48>	U18	D48	
_MAXBUS_DATA<49>	W17	D49	
_MAXBUS_DATA<50>	W18	D50	
_MAXBUS_DATA<51>	T16	D51	
_MAXBUS_DATA<52>	T18	D52	
_MAXBUS_DATA<53>	T17	D53	
_MAXBUS_DATA<54>	W3	D54	
_MAXBUS_DATA<55>	V17	D55	
_MAXBUS_DATA<56>	U4	D56	
_MAXBUS_DATA<57>	U8	D57	
_MAXBUS_DATA<58>	U7	D58	
_MAXBUS_DATA<59>	R7	D59	
_MAXBUS_DATA<60>	P6	D60	
_MAXBUS_DATA<61>	R8	D61	
_MAXBUS_DATA<62>	W8	D62	
_MAXBUS_DATA<63>	T8	D63	

Signal	Pin	Signal	Pin
		DP0	T3 NC
		DP1	W4 NC
		DP2	T4 NC
		DP3	W9 NC
		DP4	M6 NC
		DP5	V3 NC
		DP6	N8 NC
		DP7	W6 NC
DBG*	M2	MAXBUS_CPU0_DBG_L	6 32
DRDY*	R3	MAXBUS_CPU0_DRDY_L_R	
DTI0	G1	MAXBUS_EDTI	33
DTI1	K1	MAXBUS_DTI<0>	9 32
DTI2	P1	MAXBUS_DTI<1>	9 32
DTI3	N1	MAXBUS_DTI<2>	9 32
TA*	K6	MAXBUS_TA_L	6 32
TEA*	L1	MAXBUS_TEA_L	6 32
HIT*	B2	MAXBUS_CPU0_HIT_L	6 32

R3600 0 5% 1/10W MF-LF 402 — PLACE RC GLITCH FILTER CLOSE TO CPU PIN

MAXBUS_CPU0_DRDY_L 6 32

C3600 10PF 5% 50V CERM 402

U3600 (1 OF 6)

BGA, XXGHZ-XXV, A0-X.X, OMIT, CRITICAL

Signal	Pin	Signal	Pin
MAXBUS_CPU0_BR_L	D2	BR*	
MAXBUS_CPU0_BG_L	M1	BG*	
MAXBUS_TS_L	L4	TS*	
CPU0_PULLDOWN	E11	A0	
	H1	A1	
	C11	A2	
	G3	A3	
MAXBUS_ADDR<0>	F10	A4	
MAXBUS_ADDR<1>	L2	A5	
MAXBUS_ADDR<2>	D11	A6	
MAXBUS_ADDR<3>	D1	A7	
MAXBUS_ADDR<4>	C10	A8	
MAXBUS_ADDR<5>	G2	A9	
MAXBUS_ADDR<6>	D12	A10	
MAXBUS_ADDR<7>	L3	A11	
MAXBUS_ADDR<8>	G4	A12	
MAXBUS_ADDR<9>	T2	A13	
MAXBUS_ADDR<10>	F4	A14	
MAXBUS_ADDR<11>	V1	A15	
MAXBUS_ADDR<12>	J4	A16	
MAXBUS_ADDR<13>	R2	A17	
MAXBUS_ADDR<14>	K5	A18	
MAXBUS_ADDR<15>	W2	A19	
MAXBUS_ADDR<16>	J2	A20	
MAXBUS_ADDR<17>	K4	A21	
MAXBUS_ADDR<18>	N4	A22	
MAXBUS_ADDR<19>	J3	A23	
MAXBUS_ADDR<20>	M5	A24	
MAXBUS_ADDR<21>	P5	A25	
MAXBUS_ADDR<22>	N3	A26	
MAXBUS_ADDR<23>	T1	A27	
MAXBUS_ADDR<24>	V2	A28	
MAXBUS_ADDR<25>	U1	A29	
MAXBUS_ADDR<26>	N5	A30	
MAXBUS_ADDR<27>	W1	A31	
MAXBUS_ADDR<28>	B12	A32	
MAXBUS_ADDR<29>	C4	A33	
MAXBUS_ADDR<30>	G10	A34	
MAXBUS_ADDR<31>	B11	A35	

R3601 470 5% 1/10W MF-LF 402

Signal	Pin	Signal	Pin
		AP0	C1 NC
		AP1	E3 NC
		AP2	H6 NC
		AP3	F5 NC
		AP4	G7 NC
		TT0	E5 MAXBUS_TT<0> 9 32
		TT1	E6 MAXBUS_TT<1> 9 32
		TT2	F6 MAXBUS_TT<2> 9 32
		TT3	E9 MAXBUS_TT<3> 9 32
		TT4	C5 MAXBUS_TT<4> 9 32
		TBST*	F11 MAXBUS_TBST_L 9 32
		TSIZ0	G6 MAXBUS_TSIZ<0> 9 32
		TSIZ1	F7 MAXBUS_TSIZ<1> 9 32
		TSIZ2	E7 MAXBUS_TSIZ<2> 9 32
		GBL*	E2 MAXBUS_GBL_L 9 32
		WT*	D3 MAXBUS_WT_L 9 32
		CI*	J1 MAXBUS_CI_L 9 32
		AACK*	R1 MAXBUS_AACK_L 6 32
		ARTRY*	N2 MAXBUS_ARTRY_L 6 32
		SHD0*	E4 MAXBUS_SHD0_L 33
		SHD1*	H5 MAXBUS_SHD1_L 33
		SYSCLK	A10 =MAXBUS_CPU0_CLK 11 33
		CLK_OUT	H2 TP_CPU0_CLKOUT ADD GND TP NEAR CLKOUT TP
		TBEN	E1 MAXBUS_TBEN 21
		QREQ*	P4 MAXBUS_CPU0_QREQ_L 32
		QACK*	G5 MAXBUS_CPU0_QACK_L 32
		CKSTP_IN*	A3
		CKSTP_OUT*	B1 CPU_CHKSTP_OUT_L 34

U3600 (5 OF 6)

BGA, XXGHZ-XXV, A0-X.X, OMIT, CRITICAL

=PP1V5R1V8_MAXBUS 34 33 32 21 10

Signal	Pin	Signal	Pin
		OVDD	B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8
		OVDD	P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14
TP_CPU0_OVDDSENSE1	E18	OVDDSENSE1	
TP_CPU0_OVDDSENSE2	G18	OVDDSENSE2	

(Kelvin sense points)

=PP1V5R1V8_MAXBUS 10 21 32 33 34

VIO DECOUPLING (28 PINS)

26 X 1UF (0402)
2 X 10UF (0603)

C3670 1uF 10% 6.3V CERM 402
C3671 1uF 10% 6.3V CERM 402
C3672 1uF 10% 6.3V CERM 402
C3673 1uF 10% 6.3V CERM 402
C3674 1uF 10% 6.3V CERM 402
C3675 1uF 10% 6.3V CERM 402
C3676 1uF 10% 6.3V CERM 402
C3677 1uF 10% 6.3V CERM 402
C3678 1uF 10% 6.3V CERM 402
C3679 1uF 10% 6.3V CERM 402
C3680 1uF 10% 6.3V CERM 402
C3681 1uF 10% 6.3V CERM 402
C3682 1uF 10% 6.3V CERM 402
C3683 1uF 10% 6.3V CERM 402
C3684 1uF 10% 6.3V CERM 402
C3685 1uF 10% 6.3V CERM 402
C3686 1uF 10% 6.3V CERM 402
C3687 1uF 10% 6.3V CERM 402
C3688 1uF 10% 6.3V CERM 402
C3689 1uF 10% 6.3V CERM 402
C3690 1uF 10% 6.3V CERM 402
C3691 1uF 10% 6.3V CERM 402
C3692 1uF 10% 6.3V CERM 402
C3693 1uF 10% 6.3V CERM 402
C3694 1uF 10% 6.3V CERM 402
C3695 1uF 10% 6.3V CERM 402
C3698 10uF 20% 4V X5R 603
C3699 10uF 20% 4V X5R 603

MAXBUS Straps

34 33 32 21 10 =PP1V5R1V8_MAXBUS

33 MAXBUS_SHD0_L — R3610 10K 5% 1/16W MF-LF 402

33 MAXBUS_SHD1_L — R3611 10K 1% 1/16W MF-LF 402

33 MAXBUS_EDTI — R3620 1K 1% 1/16W MF-LF 402

A8 MaxBus (CPU0)	
SYNC_MASTER=MARIAS	SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 36 OF 115	

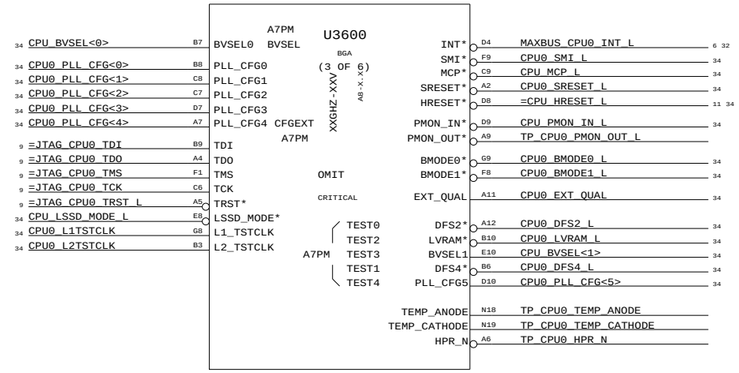
Page Notes

Power aliases required by this page:
- =PP1V5R1V8_MAXBUS
- =PP3V3_PWRON_PLLSEL

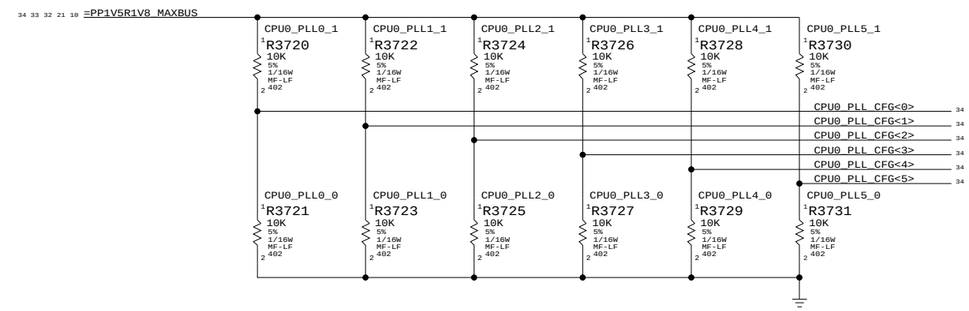
Signal aliases required by this page:
- =CPU0_JTAG_TDI
- =CPU0_JTAG_TDO
- =CPU0_JTAG_TMS
- =CPU0_JTAG_TCK
- =CPU0_JTAG_TRST_L
- =CPU_HRESET_L (Reset given to all processors)

BOM options provided by this page:
- CPU_PLL0_0/1
- CPU0_PLL1_0/1
- CPU0_PLL2_0/1
- CPU0_PLL3_0/1
- CPU0_PLL4_0/1
- CPU0_PLL5_0/1

These must be selected to set the CPU core to Maxbus frequency ratio to attain the desired spec
- MAXBUS_1V5 - MAXBUS_1V8
 One of these must be selected to set the Maxbus voltage
 * the MAXBUS_1V5 option does not exist for A7PM
- CPU_A7PM - CPU_A8
 One of these must be selected to ensure the the above strap is interpreted correctly



CPU0 PLL CONFIG CIRCUITRY



BUS TYPE SELECT

SIGNAL	TIED	MODE
CPU0_BMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE

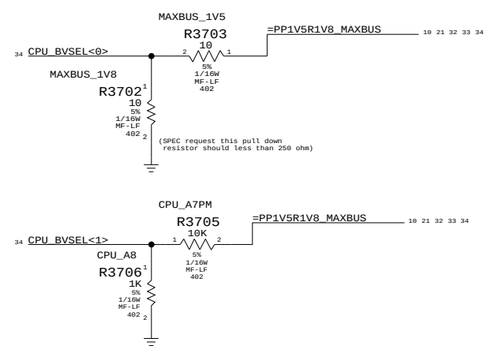
A7PM

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
2.5V INTERFACE	CPU_HRESET_L	OVDD
RESERVED(1.5V)	CPU_HRESET_INV	OVDD

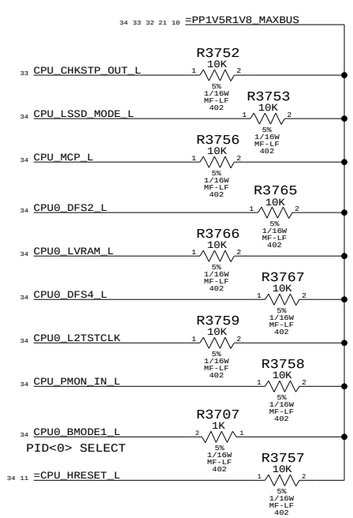
A8

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	GND
1.5V INTERFACE	OVDD	GND
RESERVED	CPU_HRESET_L	GND
RESERVED	CPU_HRESET_INV	GND
2.5V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
RESERVED	CPU_HRESET_L	OVDD
RESERVED	CPU_HRESET_INV	OVDD

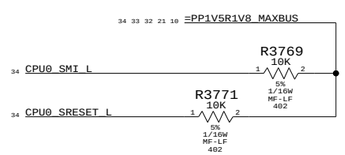
MAXBUS VSEL



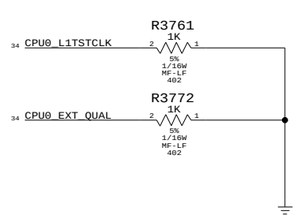
CPU PULLUPS



INTERRUPT PULL-UPS



CPU PULLDOWNS



CPU0 FREQUENCY CONFIGURATION

() Indicates DFS setting supported by A8 only

BOM GROUP	DFS SUPPORT F/2	DFS SUPPORT F/4	PLL BITS 012345	BOM OPTIONS
CPU0_BUSRATIO_1.0X	-	-	001100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_2.0X	-	-	010000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_3.0X	-	-	100000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_4.0X	2.0X	-	101000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.0X	2.5X	-	101100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.5X	(2.75X)	-	100100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.0X	3.0X	-	110100	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.5X	(3.25X)	-	010100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.0X	3.5X	-	001000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.5X	(3.75X)	-	000100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.0X	4.0X	2.0X	110000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.5X	(4.25X)	-	011000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_9.0X	4.5X	(2.25X)	011110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_9.5X	(4.75X)	-	011100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_10.0X	5.0X	2.5X	101010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_10.5X	(5.25X)	-	100010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.0X	5.5X	(2.75X)	100110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.5X	(5.75X)	-	000000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_12.0X	6.0X	3.0X	101110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_12.5X	(6.25X)	-	111110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.0X	6.5X	(3.25X)	010110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.5X	(6.75X)	-	111000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_14.0X	7.0X	3.5X	110010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_15.0X	7.5X	(3.75X)	000110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_16.0X	8.0X	4.0X	110110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_17.0X	8.5X	(4.25X)	000010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_18.0X	9.0X	4.5X	001010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_20.0X	10.0X	5.0X	001110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_21.0X	10.5X	(5.25X)	010010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_24.0X	12.0X	6.0X	011010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_28.0X	14.0X	7.0X	111010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0

A8 Configuration Straps

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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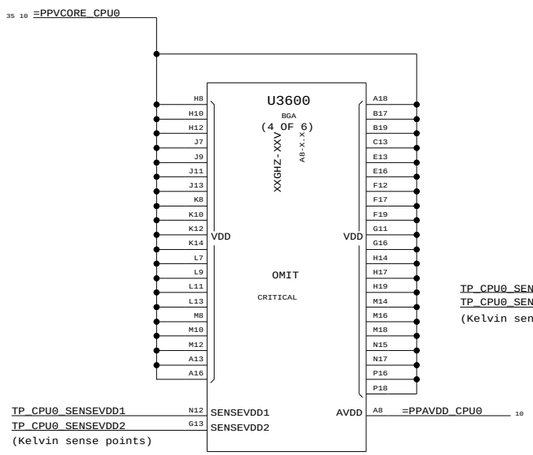
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 37 OF 115	

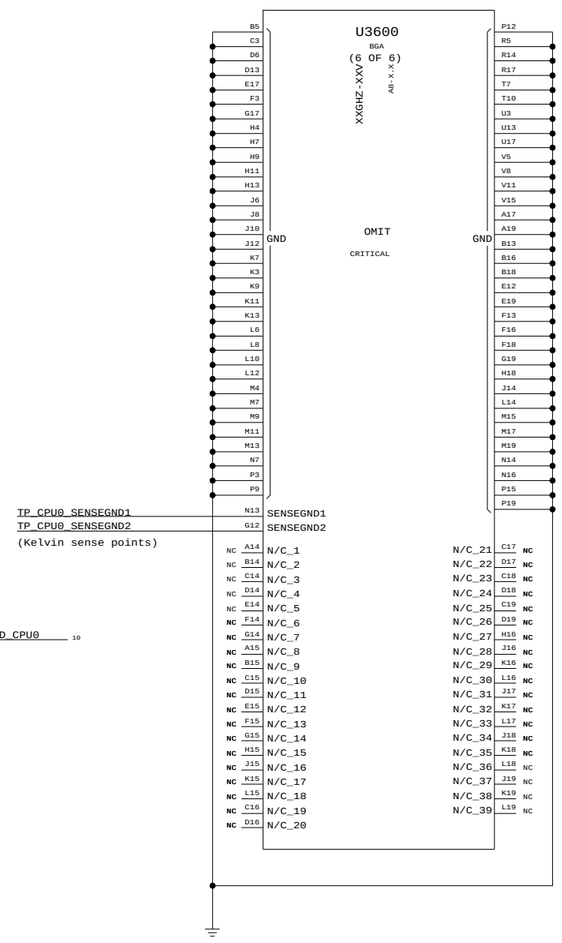
Page Notes

Power aliases required by this page:
- =PPVCORE_CPU0

Signal aliases required by this page:
(NONE)

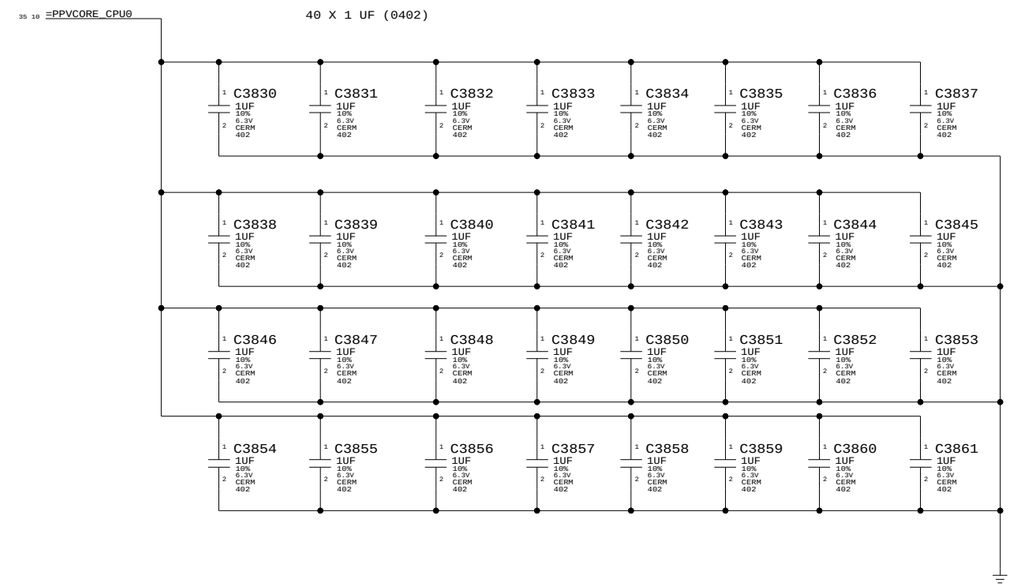
BOM options provided by this page:
(NONE)



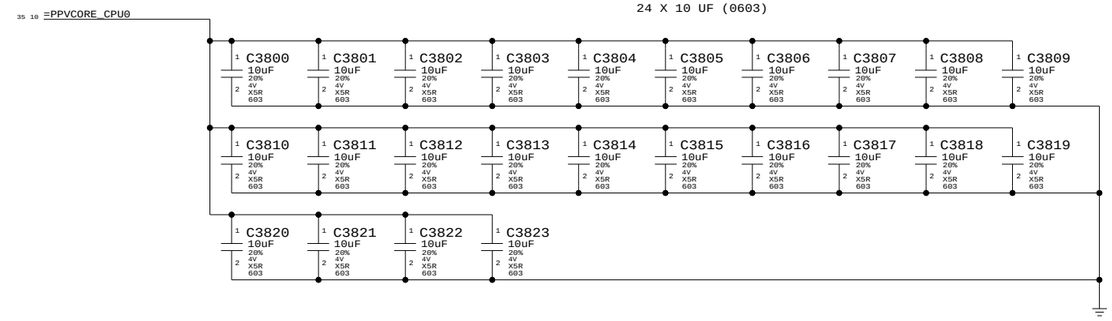


VCORE BULK CAPS

40 X 1 UF (0402)



24 X 10 UF (0603)



A8 Power (CPU0)

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 38 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
Edge	THERM	THERM	VCORE_SNS
Edge	THERM	THERM	VCORE_GNDSNS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0270	1	RES,3.48K,1%,1/16W,MF-LF,402,SMD	R3946	CPU0_VCORE_1V22
114S0258	1	RES,2.61K,1%,1/16W,MF-LF,402,SMD	R3944	CPU0_VCORE_1V22
114S0246	1	RES,2.0K,1%,1/16W,MF-LF,402,SMD	R3946	CPU0_VCORE_1V28
114S0294	1	RES,6.04K,1%,1/16W,MF-LF,402,SMD	R3944	CPU0_VCORE_1V28
114S0276	1	RES,4.02K,1%,1/16W,MF-LF,402,SMD	R3946	CPU0_VCORE_1V30
114S0254	1	RES,2.43K,1%,1/16W,MF-LF,402,SMD	R3944	CPU0_VCORE_1V30
114S0246	1	RES,2.0K,1%,1/16W,MF-LF,402,SMD	R3946	CPU0_VCORE_1V33
114S0294	1	RES,6.04K,1%,1/16W,MF-LF,402,SMD	R3944	CPU0_VCORE_1V33

(WITH VCORE OFFSET)

1.5GHZ 1.260V -> 0.940V (CPU SPEC: 1.220V -> 0.930V)

1.67GHZ 1.320V -> 0.940V (CPU SPEC: 1.280V -> 0.930V)

1.67GHZ 1.340V -> 0.940V (CPU SPEC: 1.300V -> 0.930V)

1.67GHZ 1.370V -> 0.940V (CPU SPEC: 1.330V -> 0.930V)

"Low" and "Mid" States

"High" State

Keep trace fat (1.00-2.54 mm) and short!!

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R3945 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

OUTPUT VOLTAGE

VDAC D4=0	VDAC D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

FMAX CONNECTOR

J3999 M-ST-SM-52465-1217

Pin	Signal
1	VCORE_GNDDIV_TEST
2	VCORE_GNDSNS_TEST
3	SYS_RESET_BUTTON_L
4	SYS_POWER_BUTTON_L
5	NC (RFU)
6	
7	
8	VCORE_VID<4>
9	VCORE_VID<3>
10	VCORE_VID<2>
11	VCORE_VID<1>
12	VCORE_VID<0>

CPU VCore Supply

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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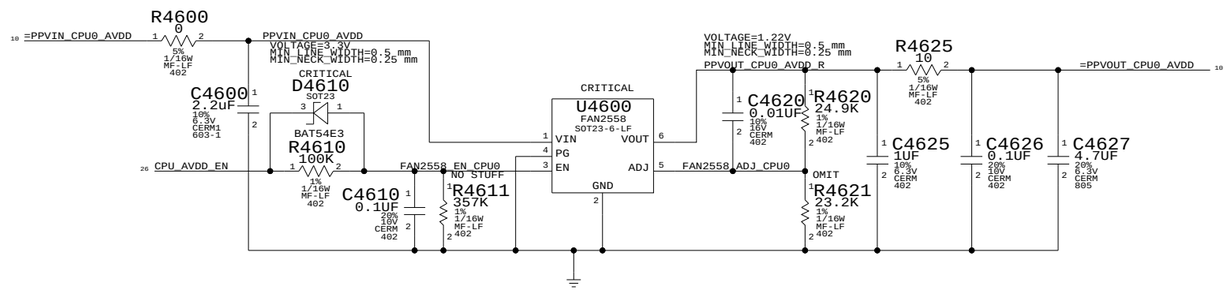
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 39 OF 115	

CPU PLL POWER SUPPLY



AVDD=0.59*(1+R4620/R4621)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0349	1	RES,23.2K,1%,1/16W,MF-LF,402,SMD	R4621	CPU0_AVDD_1V22
114S0346	1	RES,21.5K,1%,1/16W,MF-LF,402,SMD	R4621	CPU0_AVDD_1V28
114S0344	1	RES,20.5K,1%,1/16W,MF-LF,402,SMD	R4621	CPU0_AVDD_1V30
114S0342	1	RES,19.6K,1%,1/16W,MF-LF,402,SMD	R4621	CPU0_AVDD_1V33

CPU AVDD Supply

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 46 OF 115	

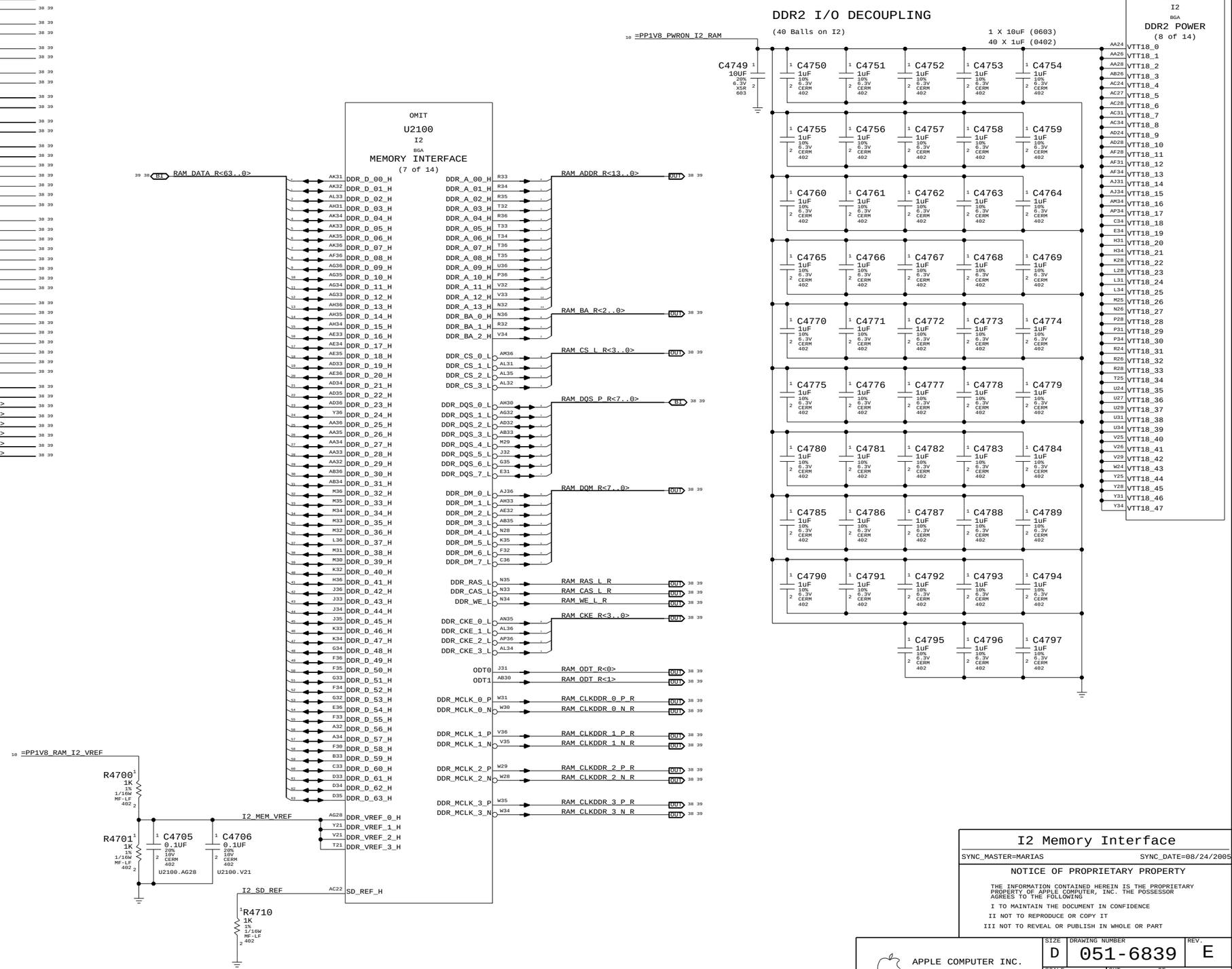
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	NET_TYPE DIFFERENTIAL_PAIR		
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_P_R	38 39
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_N_R	38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_P_R	38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_N_R	38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_P_R	38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_N_R	38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_P_R	38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_N_R	38 39
RAM_CKE_0	RAM	RAM		RAM_CKE_R<1..0>	38 39
RAM_CKE_1	RAM	RAM		RAM_CKE_R<3..2>	38 39
RAM_CS_0	RAM	RAM		RAM_CS_L_R<1..0>	38 39
RAM_CS_1	RAM	RAM		RAM_CS_L_R<3..2>	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_ADDR_R<13..0>	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_BA_R<2..0>	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_RAS_L_R	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_CAS_L_R	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_WE_L_R	38 39
RAM_ODT0	RAM	RAM		RAM_ODT_R<0>	38 39
RAM_ODT1	RAM	RAM		RAM_ODT_R<1>	38 39
RAM_DQS0	RAM	RAM		RAM_DQS_P_R<0>	38 39
RAM_DQS1	RAM	RAM		RAM_DQS_P_R<1>	38 39
RAM_DQS2	RAM	RAM		RAM_DQS_P_R<2>	38 39
RAM_DQS3	RAM	RAM		RAM_DQS_P_R<3>	38 39
RAM_DQS4	RAM	RAM		RAM_DQS_P_R<4>	38 39
RAM_DQS5	RAM	RAM		RAM_DQS_P_R<5>	38 39
RAM_DQS6	RAM	RAM		RAM_DQS_P_R<6>	38 39
RAM_DQS7	RAM	RAM		RAM_DQS_P_R<7>	38 39
RAM_DQM0	RAM	RAM		RAM_DQM_R<0>	38 39
RAM_DQM1	RAM	RAM		RAM_DQM_R<1>	38 39
RAM_DQM2	RAM	RAM		RAM_DQM_R<2>	38 39
RAM_DQM3	RAM	RAM		RAM_DQM_R<3>	38 39
RAM_DQM4	RAM	RAM		RAM_DQM_R<4>	38 39
RAM_DQM5	RAM	RAM		RAM_DQM_R<5>	38 39
RAM_DQM6	RAM	RAM		RAM_DQM_R<6>	38 39
RAM_DQM7	RAM	RAM		RAM_DQM_R<7>	38 39
RAM_DATA_0	RAM	RAM		RAM_DATA_R<7..0>	38 39
RAM_DATA_1	RAM	RAM		RAM_DATA_R<15..8>	38 39
RAM_DATA_2	RAM	RAM		RAM_DATA_R<23..16>	38 39
RAM_DATA_3	RAM	RAM		RAM_DATA_R<31..24>	38 39
RAM_DATA_4	RAM	RAM		RAM_DATA_R<39..32>	38 39
RAM_DATA_5	RAM	RAM		RAM_DATA_R<47..40>	38 39
RAM_DATA_6	RAM	RAM		RAM_DATA_R<55..48>	38 39
RAM_DATA_7	RAM	RAM		RAM_DATA_R<63..56>	38 39

Page Notes

Power aliases required by this page:
- =PP1V8_PWRON_I2_RAM
- =PP1V8_RAM_I2_VREF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 Memory Interface

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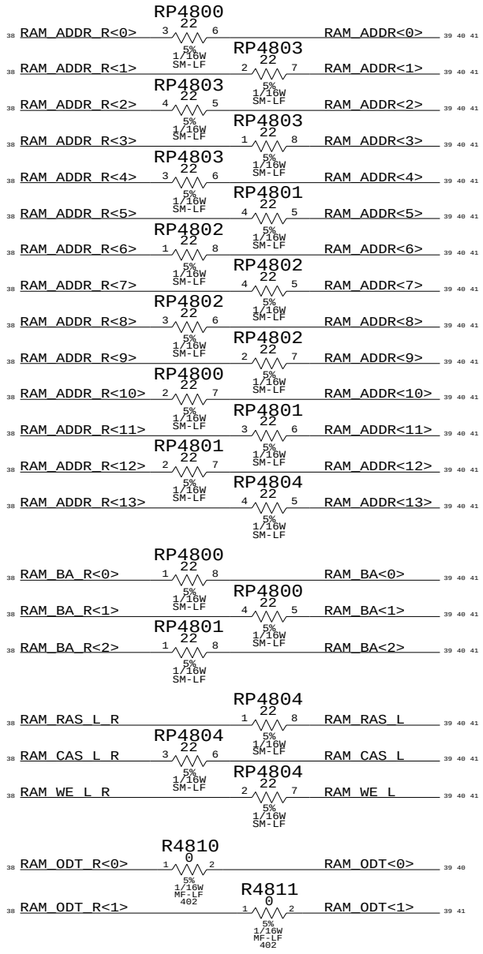
D	051-6839	E
SCALE NONE	SHT 47 OF 115	

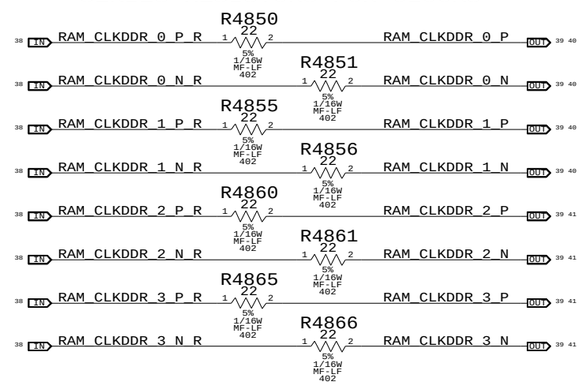
Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

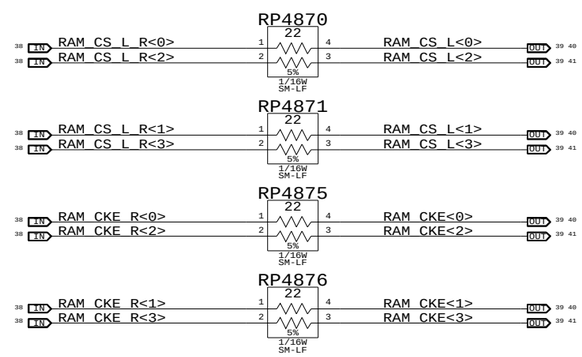


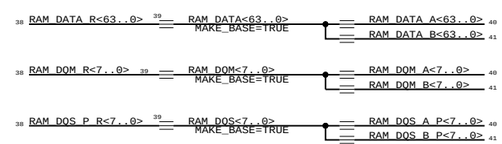
SERIES RESISTORS FOR CLOCKS

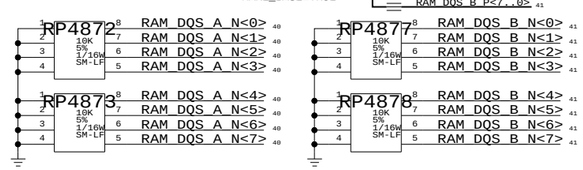


SERIES RESISTORS FOR CS / CKE

Do not swap with other RPAKs







ECSETs provided by memory controller.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	NET_TYPE DIFFERENTIAL_PAIR	
I189	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_P 39 40
I190	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_N 39 40
I192	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_P 39 40
I193	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_N 39 40
I197	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_P 39 41
I198	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_N 39 41
I199	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_P 39 41
I200	RAM_DIFF	RAM_DIFF	RAM_CLK_4	RAM_CLKDDR_3_N 39 41
I205	RAM	RAM		RAM_CKE<3..0> 39 40 41
I204	RAM	RAM		RAM_CS_L<3..0> 39 40 41
I203	RAM	RAM		RAM_ADDR<13..0> 39 40 41
I202	RAM	RAM		RAM_BA<2..0> 39 40 41
I201	RAM	RAM		RAM_RAS_L 39 40 41
I208	RAM	RAM		RAM_CAS_L 39 40 41
I207	RAM	RAM		RAM_WE_L 39 40 41
I209	RAM	RAM		RAM_ODT<1..0> 39 40 41
I206	RAM	RAM		RAM_DQS<7..0> 39
I208	RAM	RAM		RAM_DOM<7..0> 39
I210	RAM	RAM		RAM_DATA<63..0> 39

Memory Series Termination

SYNC_MASTER=MARIAS-NDIFF SYNC_DATE=N/A

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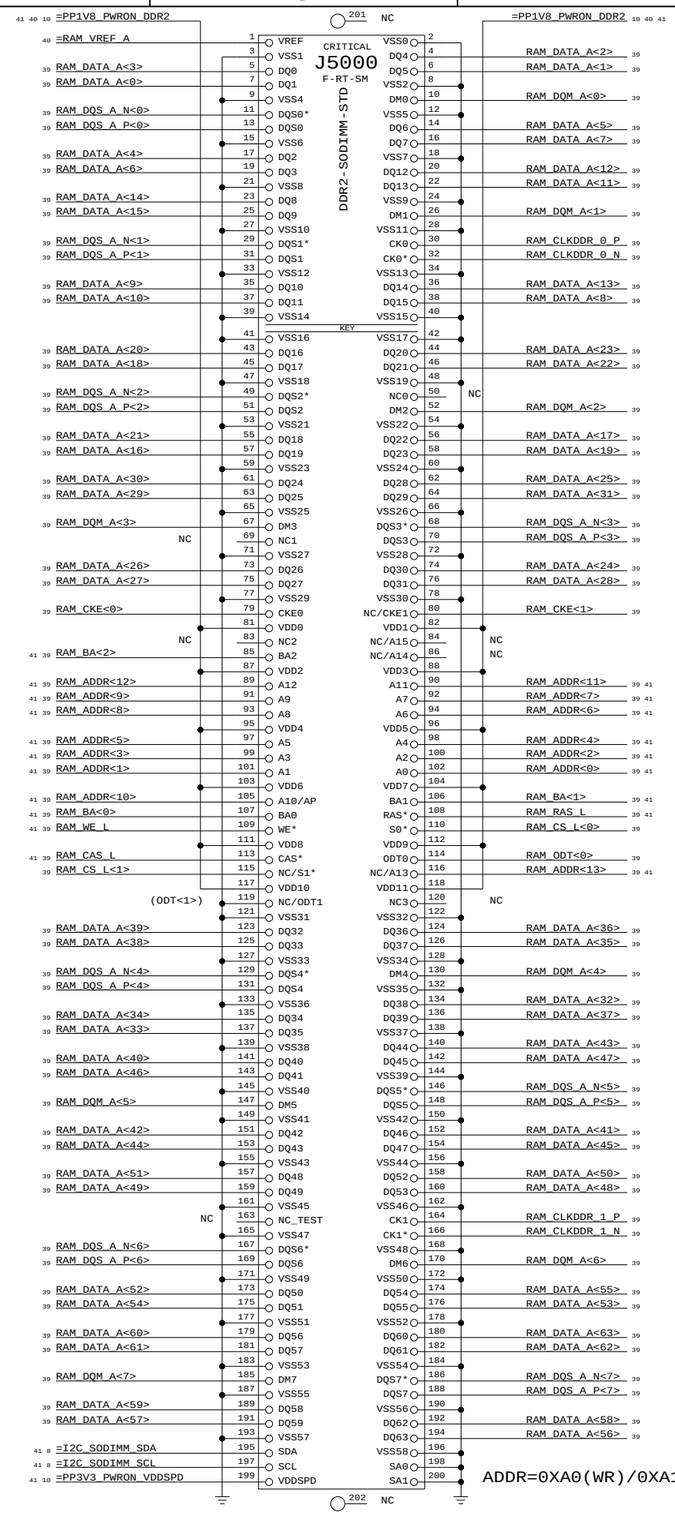
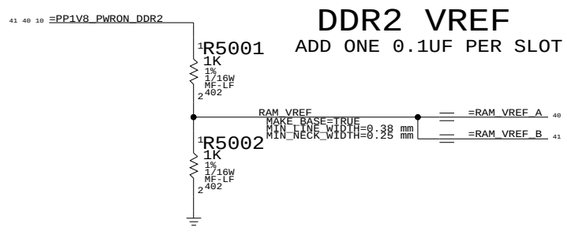
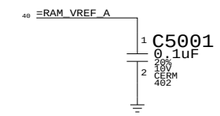


SLOT "A"
UPPER/STD SLOT
FACTORY SLOT

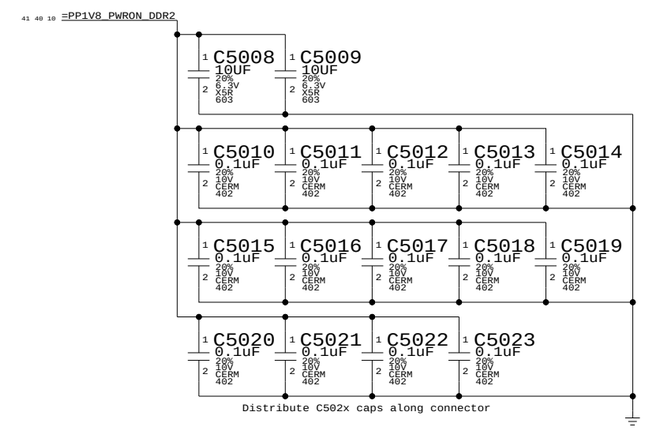
DDR2 VREF
ADD ONE 0.1UF PER SLOT



DDR2 VREF
ONE 0.1UF PER SLOT



DDR2 BYPASS
SLOT "A"



Distribute C502x caps along connector

DDR2 SO-DIMM Slot A

SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

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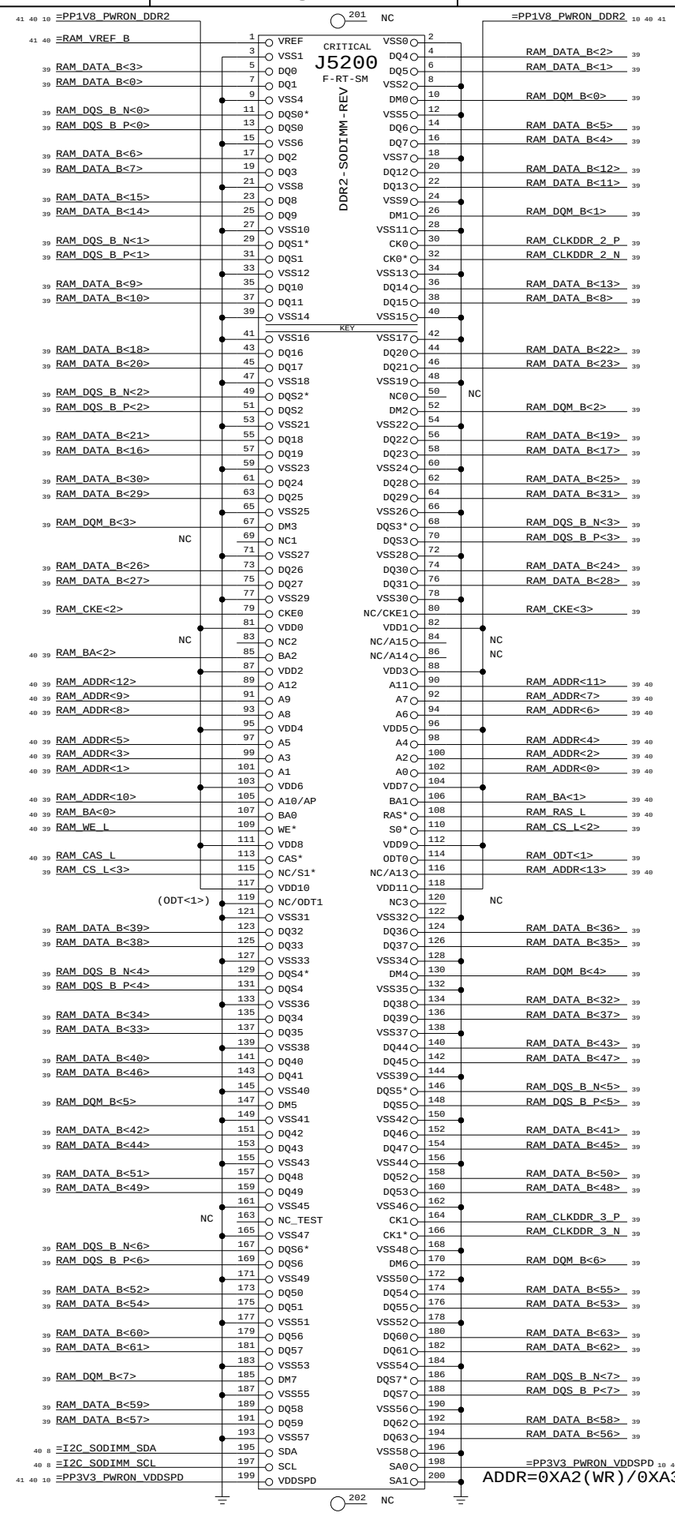
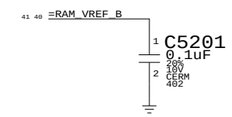
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 50 OF 115	

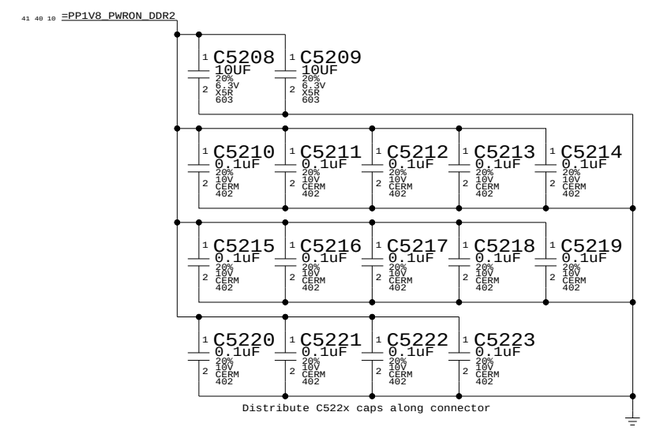
SLOT "B"
LOWER/REV SLOT
CUSTOMER SLOT



DDR2 VREF
ONE 0.1UF PER SLOT



DDR2 BYPASS
SLOT "B"



Distribute C522x caps along connector

DDR2 SO-DIMM Slot B

SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

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D	051-6839	E
SCALE NONE	SHT 52 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
FB_A_CLK_0	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_P_R	48
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_N_R	48
FB_A_CLK_1	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_P_R	48
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_N_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CKE_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CS_L_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_ADDR_R<12..0>	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_BA_R<2..0>	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_RAS_L_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CAS_L_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_WE_L_R	48
FB_A_DQS0	RAM	RAM		FB_A_DQS_R<0>	48
FB_A_DQS1	RAM	RAM		FB_A_DQS_R<1>	48
FB_A_DQS2	RAM	RAM		FB_A_DQS_R<2>	48
FB_A_DQS3	RAM	RAM		FB_A_DQS_R<3>	48
FB_A_DQS4	RAM	RAM		FB_A_DQS_R<4>	48
FB_A_DQS5	RAM	RAM		FB_A_DQS_R<5>	48
FB_A_DQS6	RAM	RAM		FB_A_DQS_R<6>	48
FB_A_DQS7	RAM	RAM		FB_A_DQS_R<7>	48
FB_A_DQM0	RAM	RAM		FB_A_DQM_R<0>	48
FB_A_DQM1	RAM	RAM		FB_A_DQM_R<1>	48
FB_A_DQM2	RAM	RAM		FB_A_DQM_R<2>	48
FB_A_DQM3	RAM	RAM		FB_A_DQM_R<3>	48
FB_A_DQM4	RAM	RAM		FB_A_DQM_R<4>	48
FB_A_DQM5	RAM	RAM		FB_A_DQM_R<5>	48
FB_A_DQM6	RAM	RAM		FB_A_DQM_R<6>	48
FB_A_DQM7	RAM	RAM		FB_A_DQM_R<7>	48
FB_A_DQ0	RAM	RAM		FB_A_DQ_R<7..0>	48
FB_A_DQ1	RAM	RAM		FB_A_DQ_R<15..8>	48
FB_A_DQ2	RAM	RAM		FB_A_DQ_R<23..16>	48
FB_A_DQ3	RAM	RAM		FB_A_DQ_R<31..24>	48
FB_A_DQ4	RAM	RAM		FB_A_DQ_R<39..32>	48
FB_A_DQ5	RAM	RAM		FB_A_DQ_R<47..40>	48
FB_A_DQ6	RAM	RAM		FB_A_DQ_R<55..48>	48
FB_A_DQ7	RAM	RAM		FB_A_DQ_R<63..56>	48

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
FB_B_CLK_0	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_P_R	48
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_N_R	48
FB_B_CLK_1	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_P_R	48
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_N_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CKE_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CS_L_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_ADDR_R<12..0>	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_BA_R<2..0>	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_RAS_L_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CAS_L_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_WE_L_R	48
FB_B_DQS0	RAM	RAM		FB_B_DQS_R<0>	48
FB_B_DQS1	RAM	RAM		FB_B_DQS_R<1>	48
FB_B_DQS2	RAM	RAM		FB_B_DQS_R<2>	48
FB_B_DQS3	RAM	RAM		FB_B_DQS_R<3>	48
FB_B_DQS4	RAM	RAM		FB_B_DQS_R<4>	48
FB_B_DQS5	RAM	RAM		FB_B_DQS_R<5>	48
FB_B_DQS6	RAM	RAM		FB_B_DQS_R<6>	48
FB_B_DQS7	RAM	RAM		FB_B_DQS_R<7>	48
FB_B_DQM0	RAM	RAM		FB_B_DQM_R<0>	48
FB_B_DQM1	RAM	RAM		FB_B_DQM_R<1>	48
FB_B_DQM2	RAM	RAM		FB_B_DQM_R<2>	48
FB_B_DQM3	RAM	RAM		FB_B_DQM_R<3>	48
FB_B_DQM4	RAM	RAM		FB_B_DQM_R<4>	48
FB_B_DQM5	RAM	RAM		FB_B_DQM_R<5>	48
FB_B_DQM6	RAM	RAM		FB_B_DQM_R<6>	48
FB_B_DQM7	RAM	RAM		FB_B_DQM_R<7>	48
FB_B_DQ0	RAM	RAM		FB_B_DQ_R<7..0>	48
FB_B_DQ1	RAM	RAM		FB_B_DQ_R<15..8>	48
FB_B_DQ2	RAM	RAM		FB_B_DQ_R<23..16>	48
FB_B_DQ3	RAM	RAM		FB_B_DQ_R<31..24>	48
FB_B_DQ4	RAM	RAM		FB_B_DQ_R<39..32>	48
FB_B_DQ5	RAM	RAM		FB_B_DQ_R<47..40>	48
FB_B_DQ6	RAM	RAM		FB_B_DQ_R<55..48>	48
FB_B_DQ7	RAM	RAM		FB_B_DQ_R<63..56>	48

M11 Frame Buffer Constraints

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SCALE NONE	SHT 55 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
AGP_CLK	CLOCK	CLOCK		AGP_CLK66M_GPU_R 11 43
I2_AGP_FBCLK	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_OUT_R 43
	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_OUT 21 43
AGP_AD_0	AGP	AGP		AGP_AD<15..0> 43 44
AGP_AD_1	AGP	AGP		AGP_AD<31..16> 43 44
AGP_AD_0	AGP	AGP		AGP_CBE_L<1..0> 43 44
AGP_AD_1	AGP	AGP		AGP_CBE_L<3..2> 43 44
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0	AGP_AD_STB0_P 43 44
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0	AGP_AD_STB0_N 43 44
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1	AGP_AD_STB1_P 43 44
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1	AGP_AD_STB1_N 43 44
AGP_SBA	AGP	AGP		AGP_SBA<7..0> 43 44
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB	AGP_SB_STB_P 43 44
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB	AGP_SB_STB_N 43 44
AGP_ST	AGP	AGP		AGP_ST<3..0> 43 44
AGP_CTL	AGP	AGP		AGP_FRAME_L 6 43 44
AGP_CTL	AGP	AGP		AGP_DEVSEL_L 6 43 44
AGP_CTL	AGP	AGP		AGP_IRDY_L 6 43 44
AGP_CTL	AGP	AGP		AGP_TRDY_L 6 43 44
AGP_CTL	AGP	AGP		AGP_STOP_L 6 43 44
AGP_PAR	AGP	AGP		AGP_PAR 43 44
AGP_DEV_CTL	AGP	AGP		AGP_PIPE_L 43
AGP_DEV_CTL	AGP	AGP		AGP_WBF_L 43 44
AGP_DEV_CTL	AGP	AGP		AGP_RBF_L 6 43 44
	AGP	AGP		AGP_REQ_L 6 43 44
	AGP	AGP		AGP_GNT_L 6 43 44

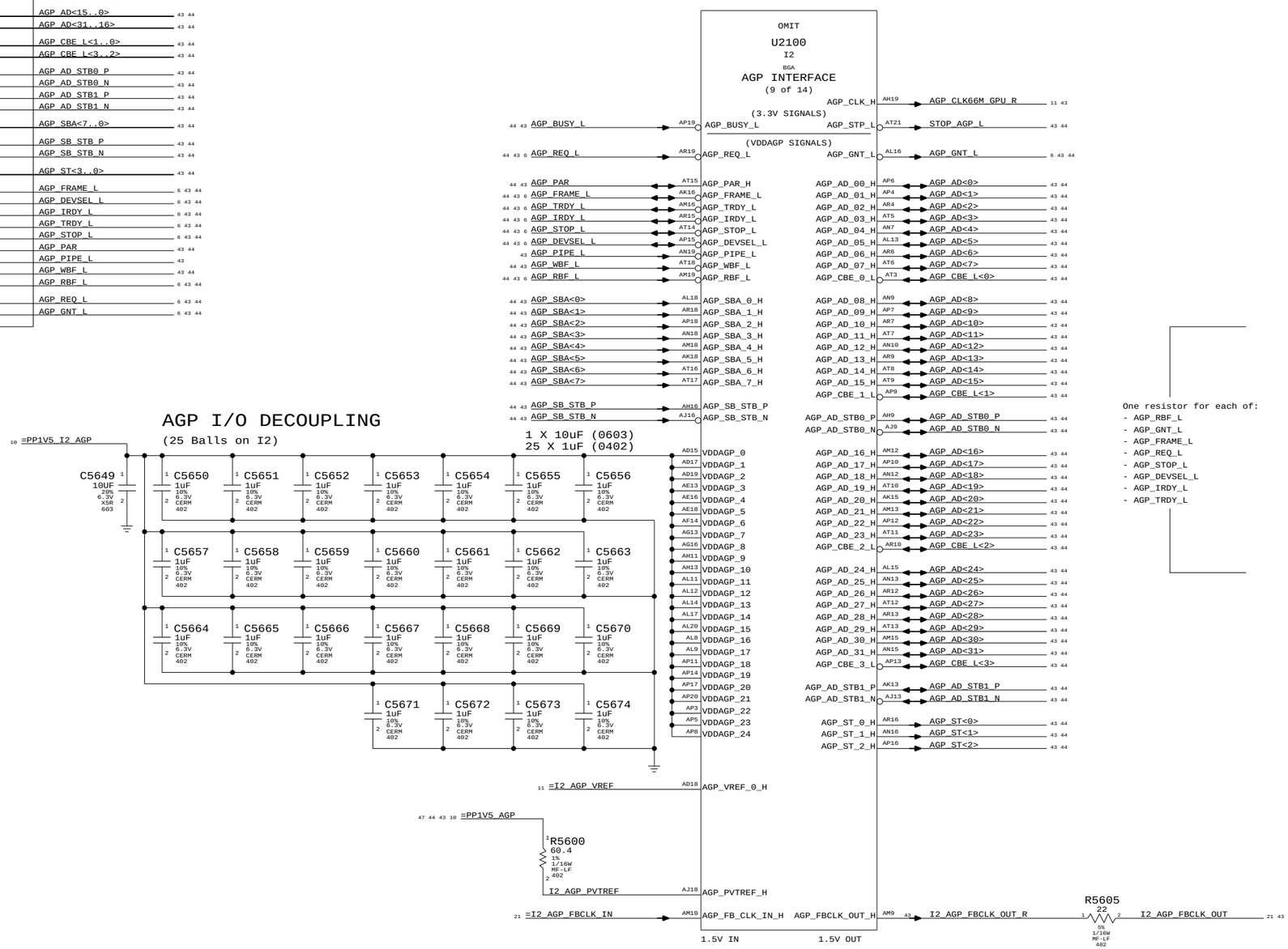
Page Notes

Power aliases required by this page:
- =PP3V3_AGP
- =PP1V5_AGP
- =PP1V5_I2_AGP

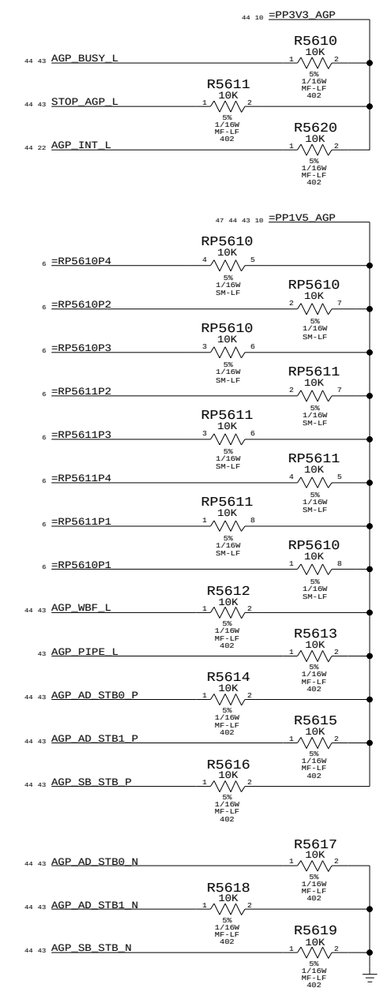
Signal aliases required by this page:
- =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
- =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

BOM options provided by this page:
(NONE)

NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.



AGP PULL-UPS/PULL DOWNS



One resistor for each of:
- AGP_RBF_L
- AGP_GNT_L
- AGP_FRAME_L
- AGP_REQ_L
- AGP_STOP_L
- AGP_DEVSEL_L
- AGP_IRDY_L
- AGP_TRDY_L

I2 AGP Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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D	051-6839	E
SCALE NONE	SHT 56 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR
LT98	CLOCK	CLOCK	

AGP_CLK66M_GPU 11 44

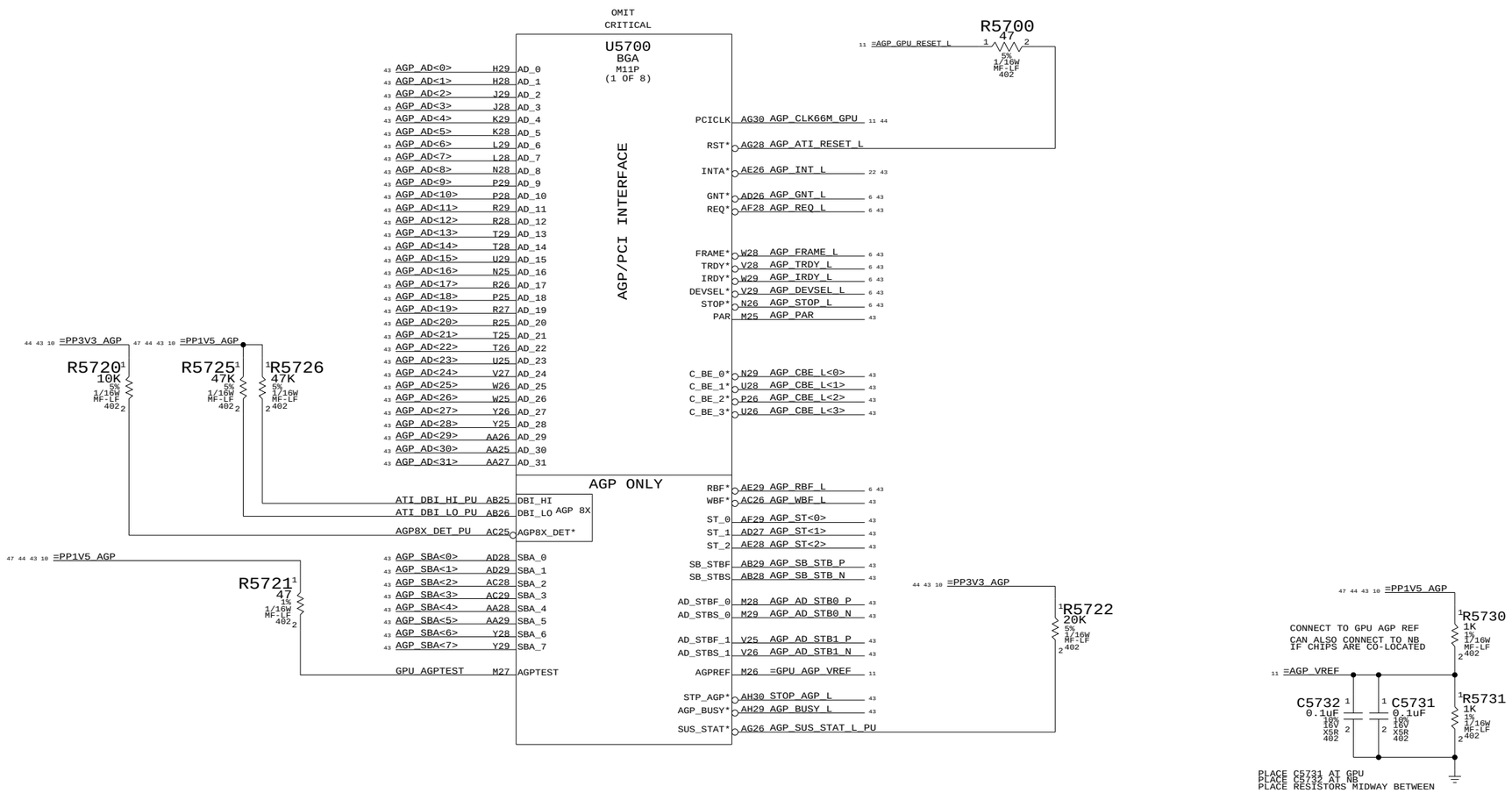
Page Notes

Power aliases required by this page:
- =PP3V3_AGP
- =PP1V5_AGP

Signal aliases required by this page:
- =AGP_VREF - VRef divider output for both GPU and NB
- =AGP_GPU_RESET_L - Active low reset for GPU

BOM options provided by this page:
(NONE)

NOTE: AGP 8x signals are not provided by this page.



GPU (M11) AGP Interface

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 57 OF 115	

Page Notes

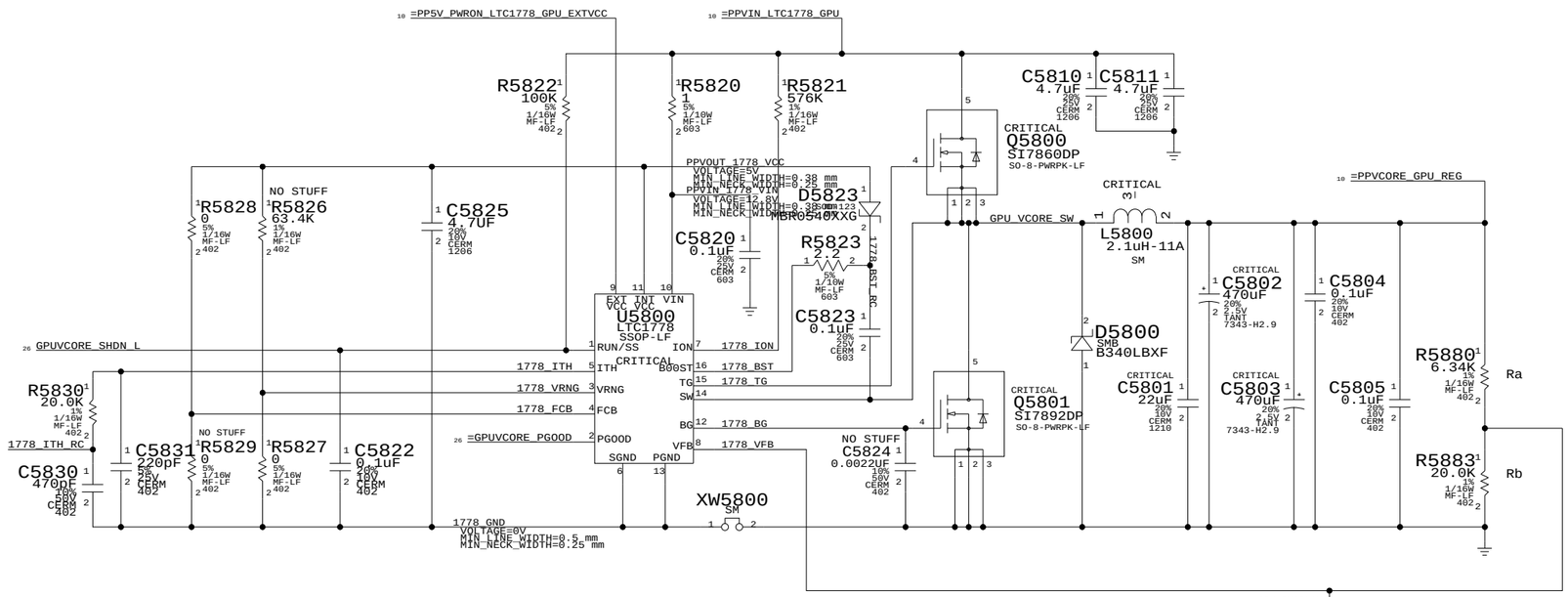
Power aliases required by this page:
- =PPVIN_LTC1778_GPU
- =PP5V_PWRON_LTC1778_GPU_EXTVCC
- =PPVCORE_GPU_REG

Signal aliases required by this page:
- =GPUVCORE_PGOOD - Active high Power Good signal for power sequencing

BOM options provided by this page:
- GPU_PWRPLAY

NOTE: Implements "Power Miser" feature for ATI GPUs

GPU VCORE SUPPLY



WHEN VCORE_CNTL HIGH => 1.307V
1.307V = 0.8V * (1 + Ra*(Rc+Rb) / (Rc*Rb))

WHEN VCORE_CNTL LOW => 1.054V
1.054V = 0.8V * (1 + Ra / Rb)

GPU VCore Supply

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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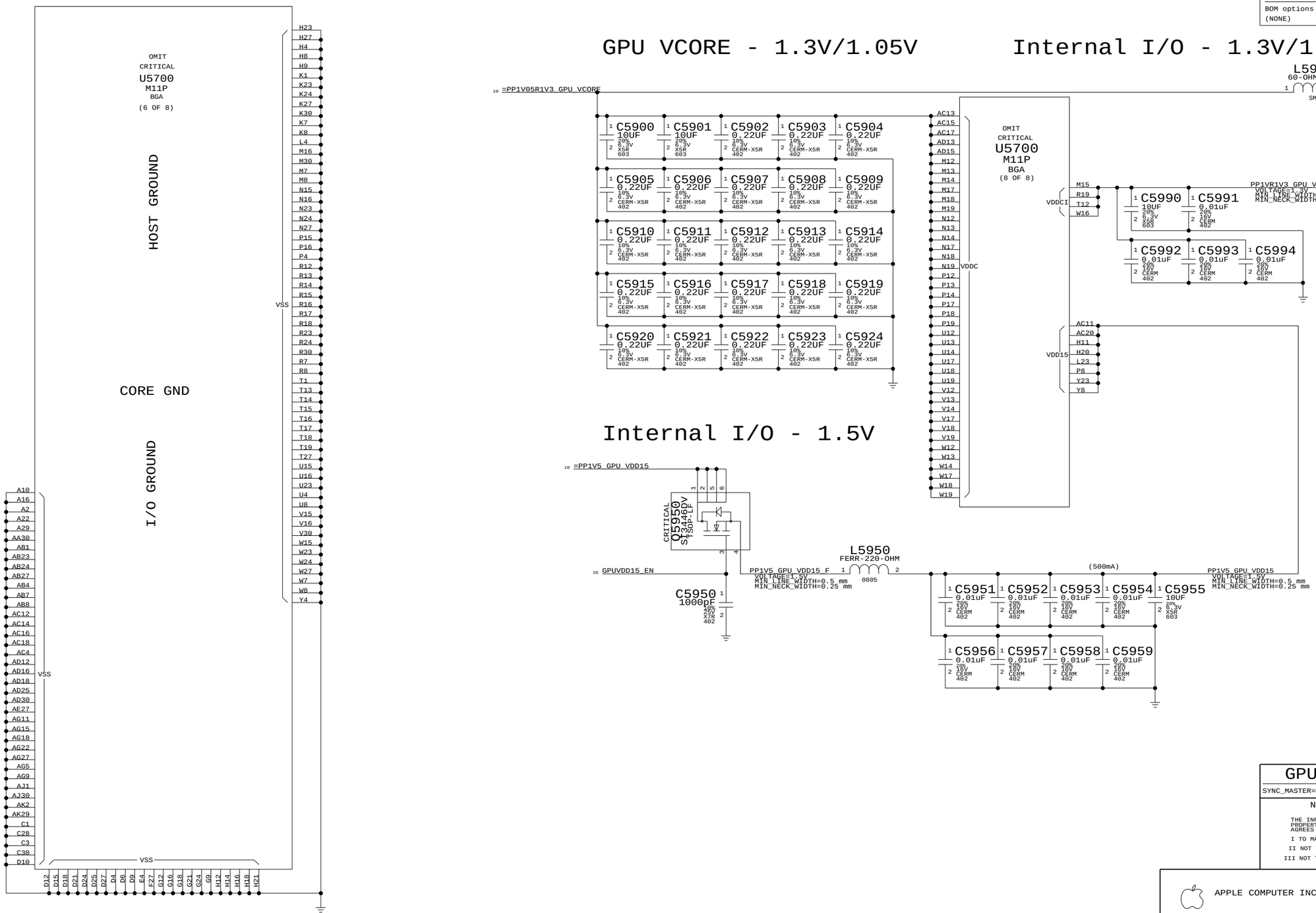
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 58 OF 115	

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GPU (M11) Core Power

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 59 OF 115	

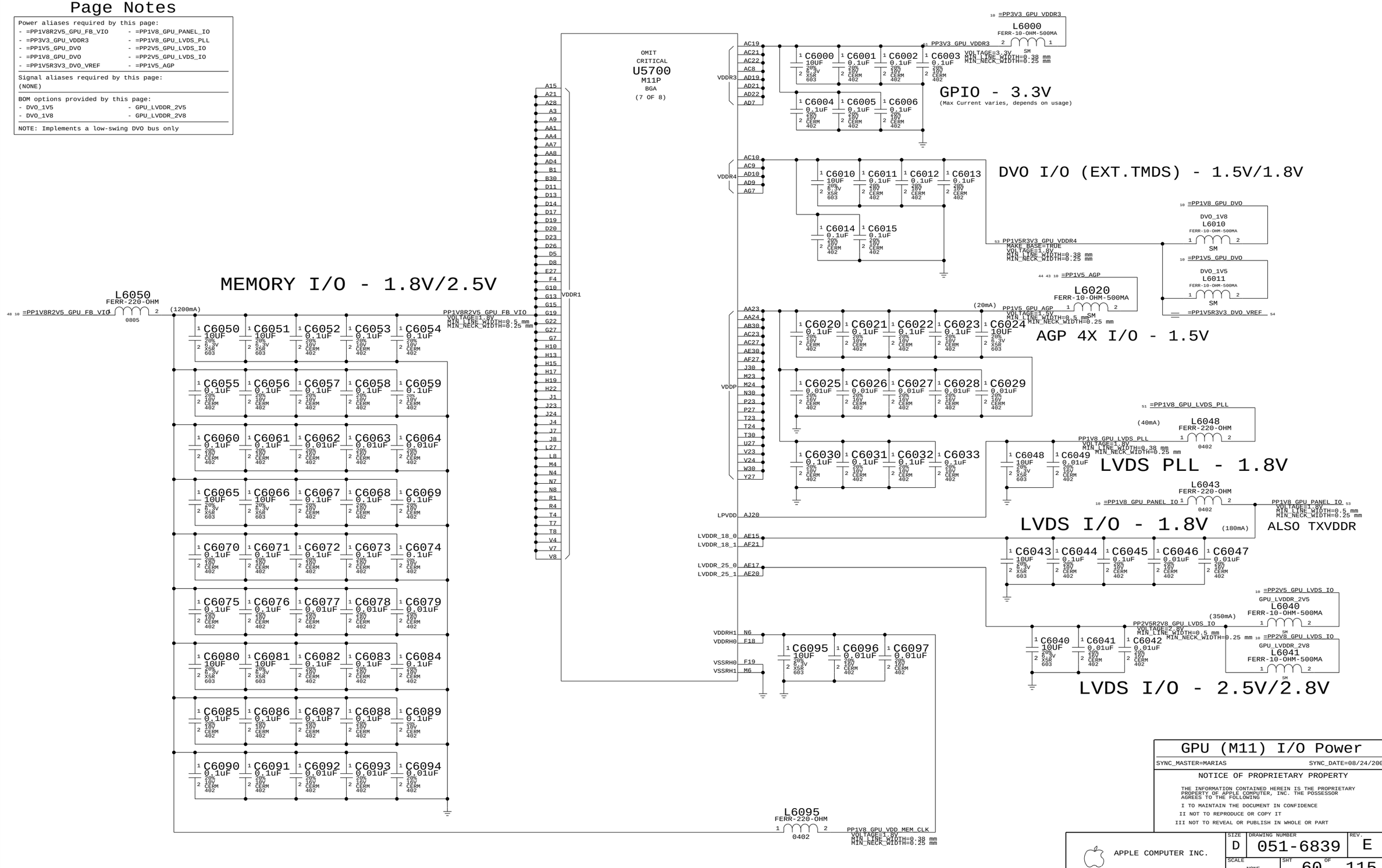
Page Notes

Power aliases required by this page:
- =PP1V8R2V5_GPU_FB_VIO
- =PP3V3_GPU_VDDR3
- =PP1V5_GPU_DVO
- =PP1V8_GPU_DVO
- =PP1V5R3V3_DVO_VREF
- =PP1V8_GPU_PANEL_IO
- =PP1V8_GPU_LVDS_PLL
- =PP2V5_GPU_LVDS_IO
- =PP2V5_GPU_LVDS_IO
- =PP1V5_AGP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- DVO_1V5
- DVO_1V8
- GPU_LVDDR_2V5
- GPU_LVDDR_2V8

NOTE: Implements a low-swing DVO bus only



GPU (M11) I/O Power

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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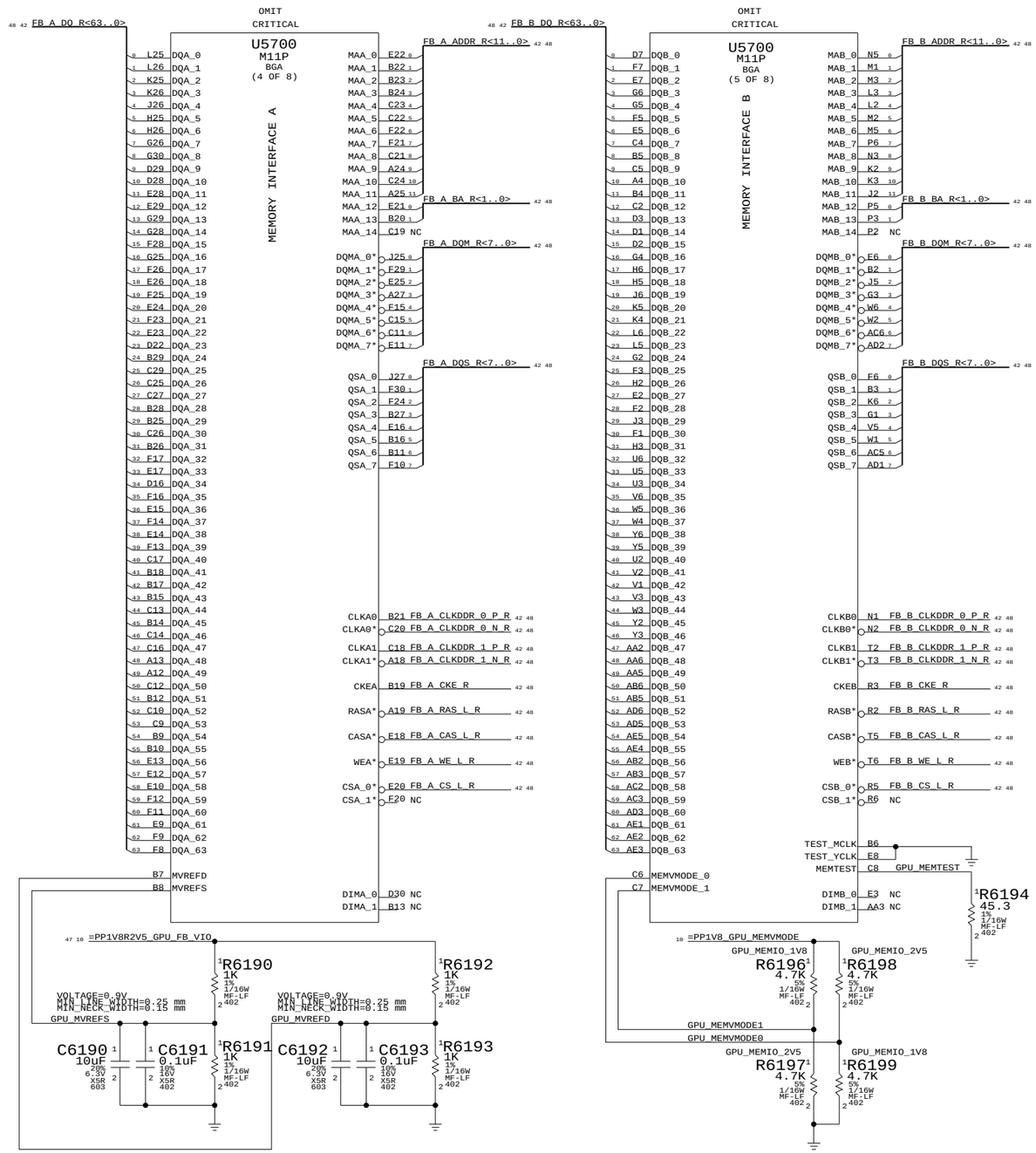
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 60 OF 115	

Page Notes

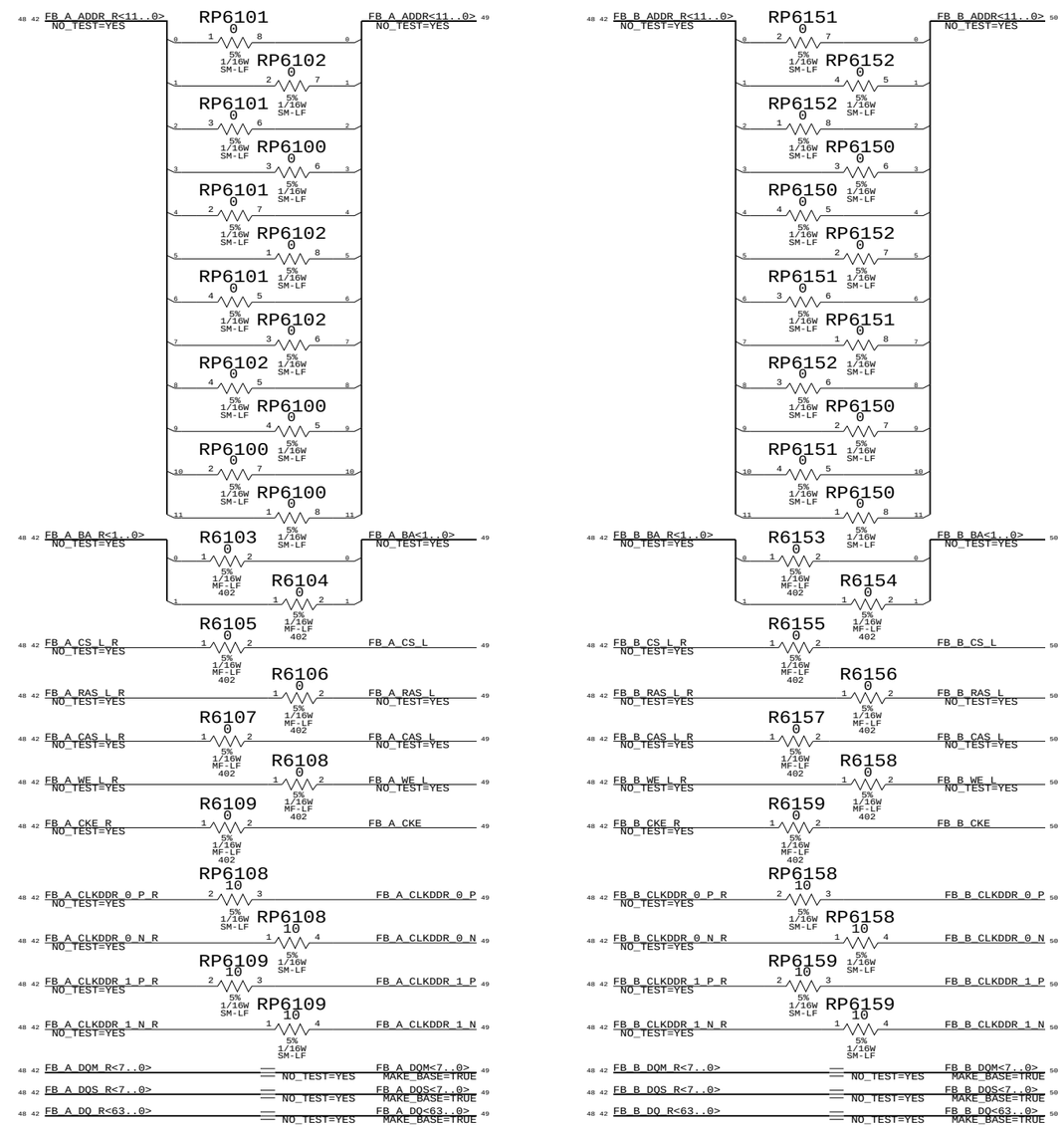
Power aliases required by this page:
- =PP1V8R2V5_GPU_FB_VIO
- =PP1V8_GPU_MEMVMODE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_MEMIO_1V8
- GPU_MEMIO_2V5



GPU Frame Buffer Series Term



GPU (M11) Frame Buffer I/F	
SYNC_MASTER=MARIAS	SYNC_DATE=08/24/2005

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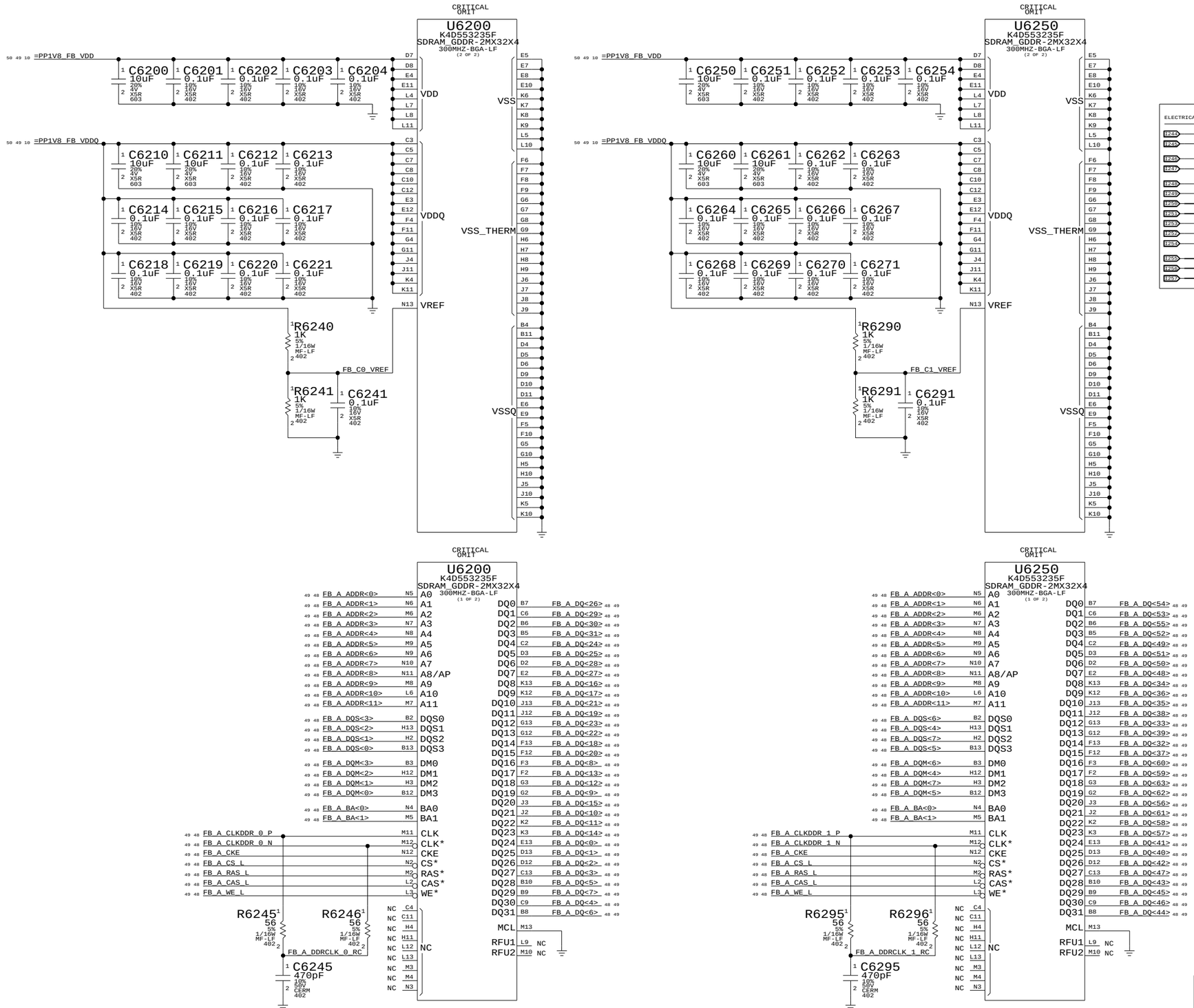
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 61 OF 115	



Page Notes

Power aliases required by this page:
- =PP1V8_FB_VDD
- =PP1V8_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
E244	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB_A_CLKDDR_0_P
E245	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB_A_CLKDDR_0_N
E246	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB_A_CLKDDR_1_P
E247	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB_A_CLKDDR_1_N
E248	RAM	RAM		FB_A_CKE
E249	RAM	RAM		FB_A_CS_L
E250	RAM	RAM		FB_A_ADDR<11..0>
E251	RAM	RAM		FB_A_BA<1..0>
E253	RAM	RAM		FB_A_RAS_L
E252	RAM	RAM		FB_A_CAS_L
E254	RAM	RAM		FB_A_WE_L
E255	RAM	RAM		FB_A_DQS<7..0>
E256	RAM	RAM		FB_A_DQM<7..0>
E257	RAM	RAM		FB_A_DQ<63..0>

ECSETs provided by GPU

GPU Frame Buffer A

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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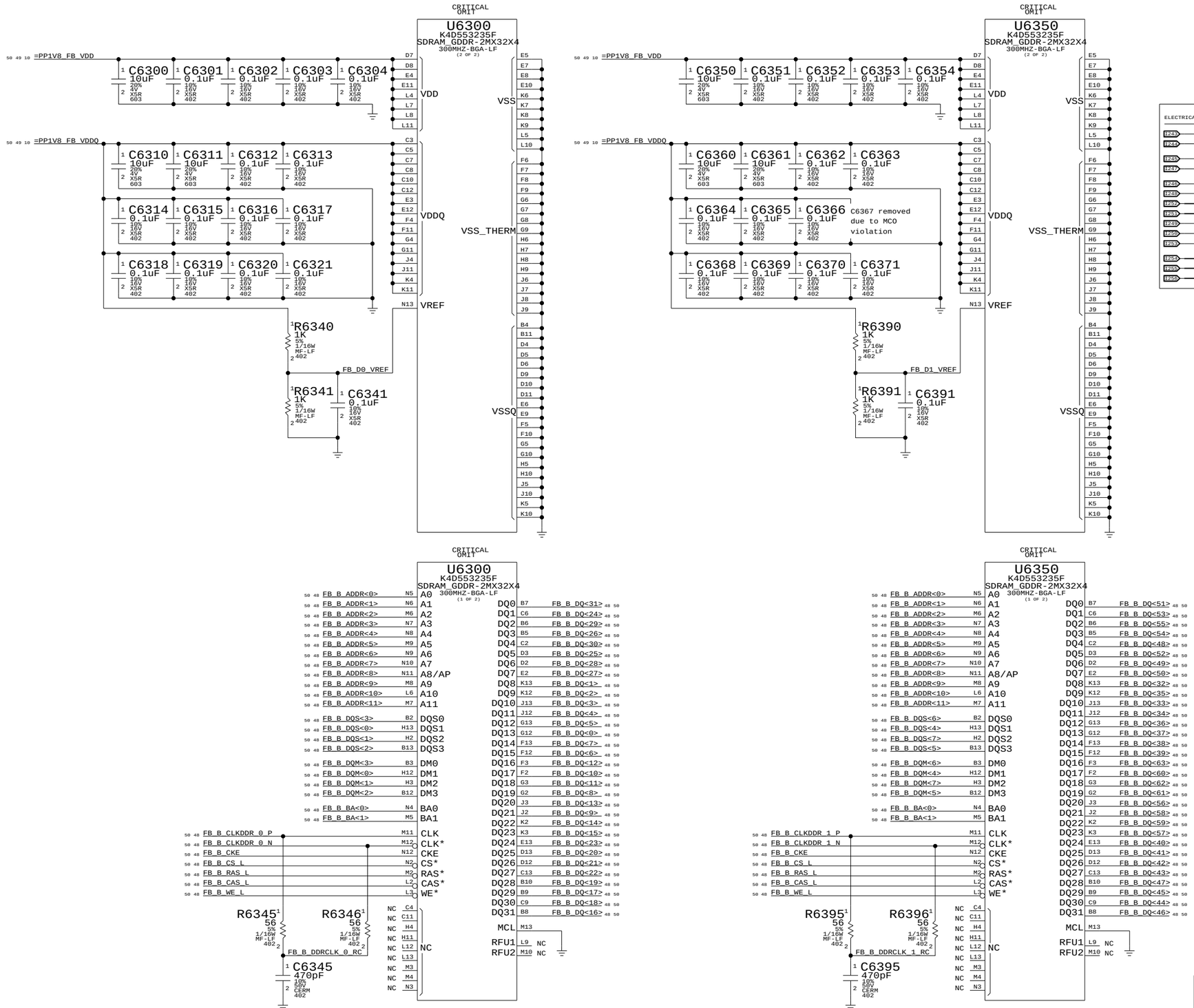
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 62 OF 115	



Page Notes

Power aliases required by this page:
- =PP1V8_FB_VDD
- =PP1V8_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
I243	RAM_DIFF	RAM_DIFF	FB_B_CLK_0	FB_B_CLKDDR_0_P 48 50
I244	RAM_DIFF	RAM_DIFF	FB_B_CLK_0	FB_B_CLKDDR_0_N 48 50
I245	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_P 48 50
I247	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_N 48 50
I246	RAM	RAM		FB_B_CKE 48 50
I248	RAM	RAM		FB_B_CS_L 48 50
I282	RAM	RAM		FB_B_ADDR<11..0> 48 50
I251	RAM	RAM		FB_B_BA<1..0> 48 50
I249	RAM	RAM		FB_B_RAS_L 48 50
I250	RAM	RAM		FB_B_CAS_L 48 50
I253	RAM	RAM		FB_B_WE_L 48 50
I254	RAM	RAM		FB_B_DQS<7..0> 48 50
I255	RAM	RAM		FB_B_DQM<7..0> 48 50
I256	RAM	RAM		FB_B_DQ<63..0> 48 50

ECSETs provided by GPU

GPU Frame Buffer B

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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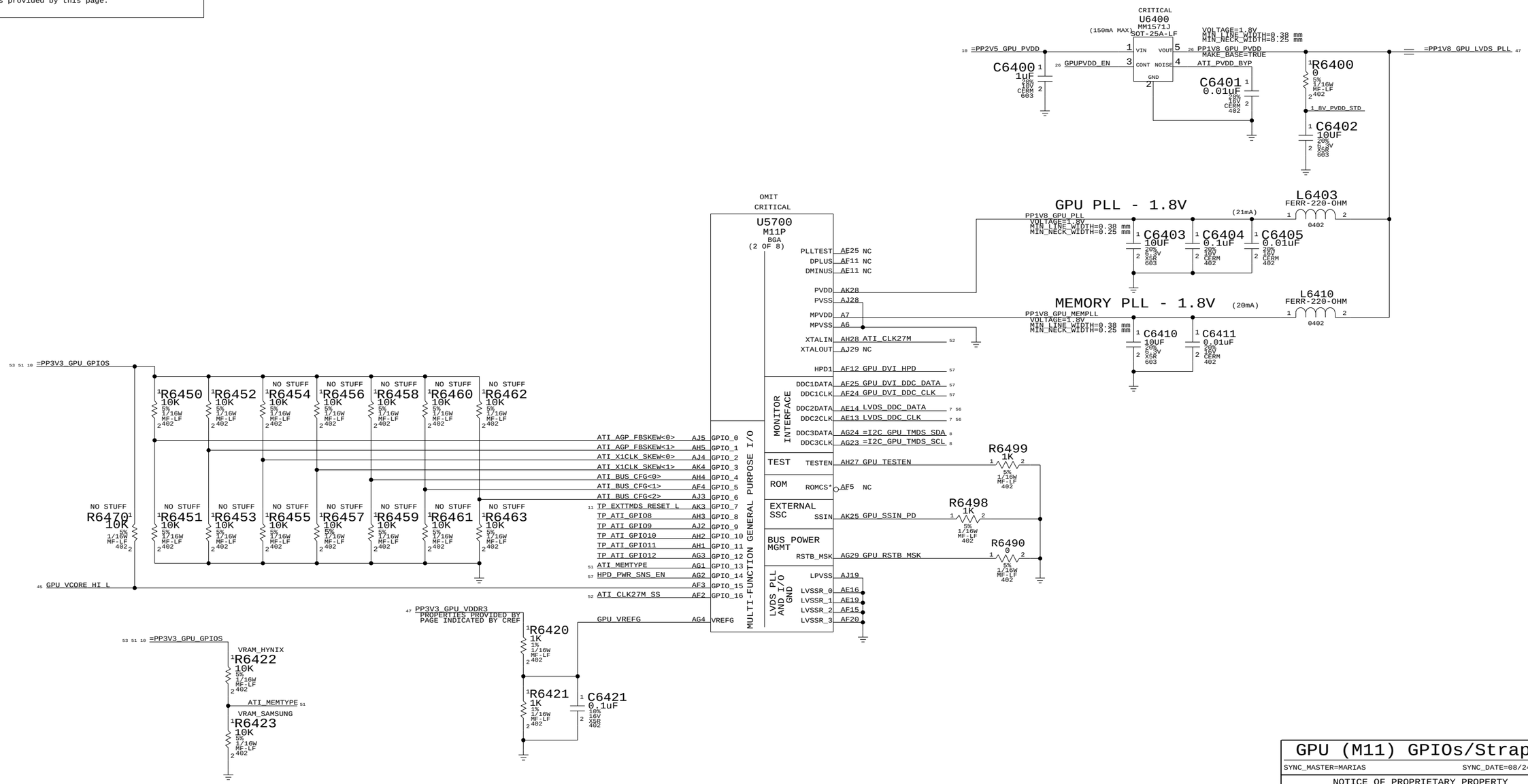
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 63 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



GPU (M11) GPIOs/Straps

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 64 OF 115	

Page Notes

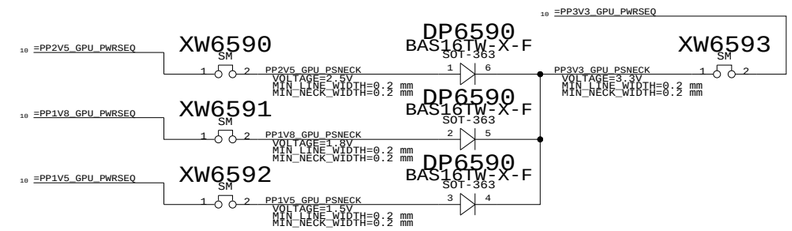
Power aliases required by this page:
- =PP3V3_GPU_CLOCKS
- =PPVIN_GPU_LVDDR_LDO
- =PP2V5_GPU_LVDDR_LDO
- =PP3V3_GPU_PWRSEQ
- =PP2V5_GPU_PWRSEQ
- =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
(NONE)

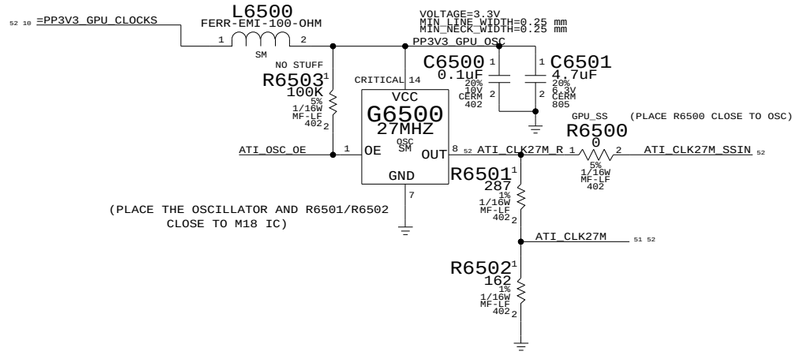
BOM options provided by this page:
- GPU_SS
- GPU_LVDDR_2V8

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
163 ATI_CLK27M	CLOCK	CLOCK		ATI_CLK27M_R 52
164	CLOCK	CLOCK		ATI_CLK27M 51 52
165	CLOCK	CLOCK		ATI_CLK27M_SSIN 52
161 ATI_CLK27M_SS	CLOCK	CLOCK		ATI_CLK27M_SS_R 52
162	CLOCK	CLOCK		ATI_CLK27M_SS 51 52

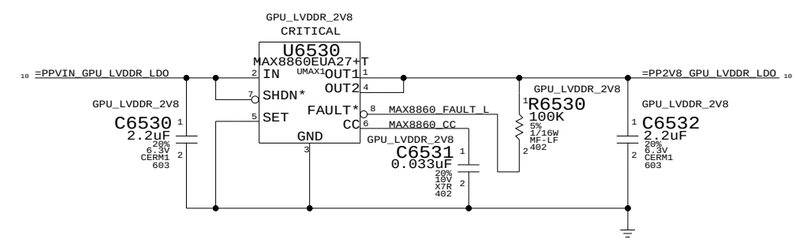
M11 Power Shutdown Sequencing



27M OSC



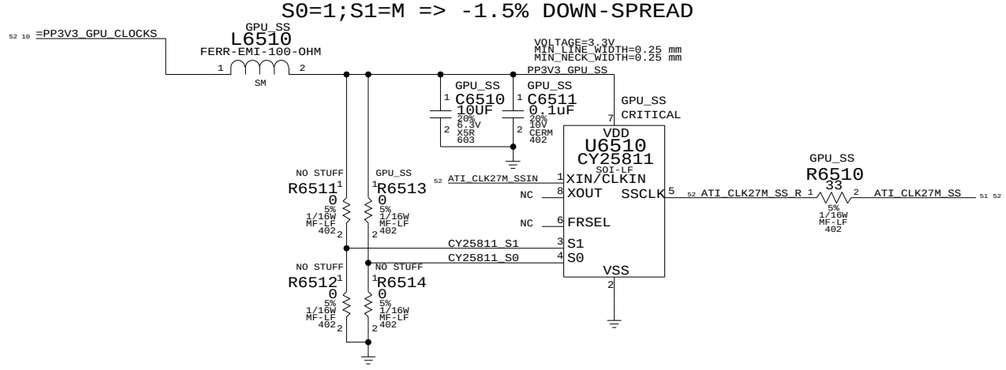
LVDDR 2.8V LDO



PART NUMBER	1S ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1188	353S1140	GPU_LVDDR_2V8	U6530	Primary is 2.77V/Alt is 2.82V

SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD



GPU (M11) Clocks/Misc

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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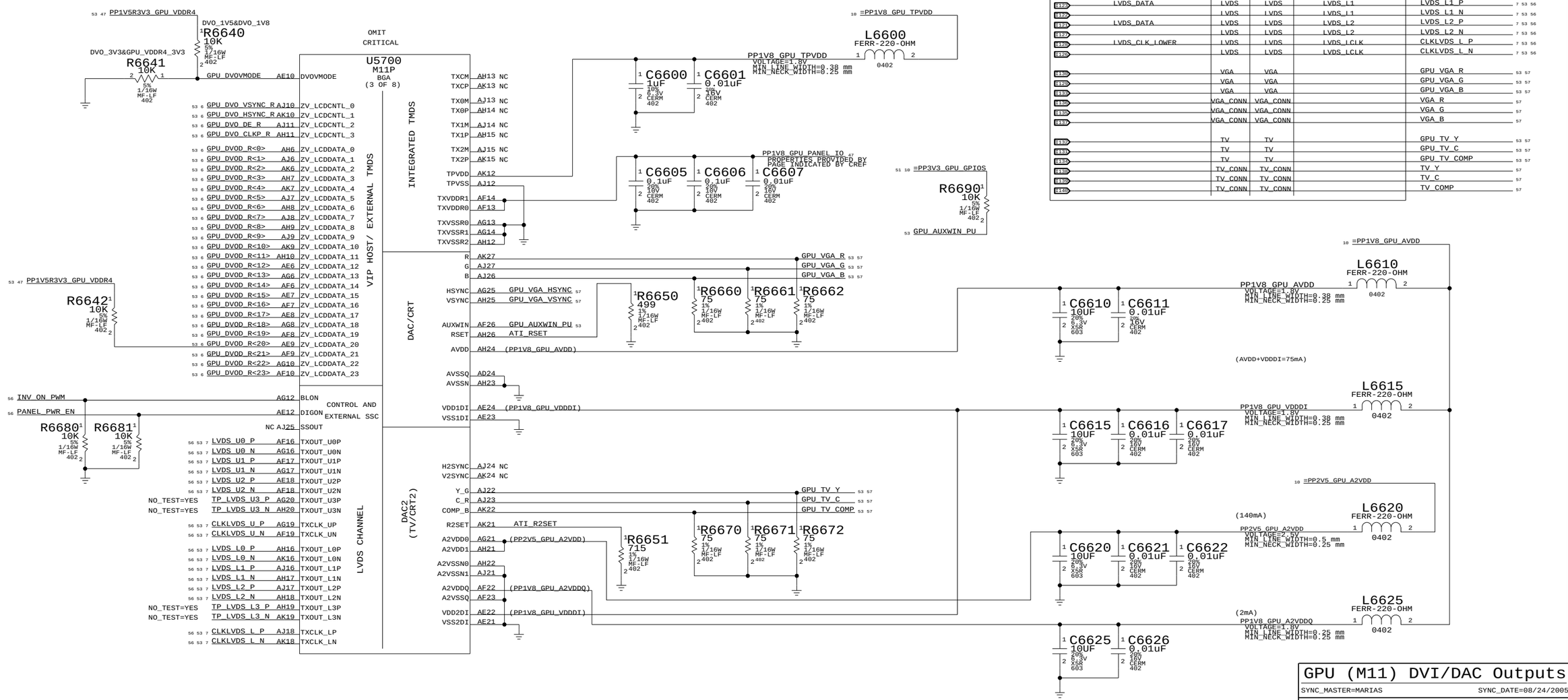
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 65 OF 115	

Page Notes

Power aliases required by this page:
- =PP2V5_GPU_A2VDD
- =PP1V8_GPU_AVDD
- =PP1V8_GPU_TPVDD
- =PP3V3_GPU_GPIOS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- DVO_1V5
- GPU_VDDR4_3V3
- DVO_1V8
- DVO_3V3



ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	DVO	DVO		GPU_DVOD_R<23..0>
ECSETs provided by SI TMDS	DVO	DVO		GPU_DVO_HSYNC_R
	DVO	DVO		GPU_DVO_VSYNC_R
	DVO	DVO		GPU_DVO_DE_R
	DVO	DVO		GPU_DVO_CLKP_R
LVDS_DATA	LVDS	LVDS	LVDS_U0	LVDS_U0_P
	LVDS	LVDS	LVDS_U0	LVDS_U0_N
LVDS_DATA	LVDS	LVDS	LVDS_U1	LVDS_U1_P
	LVDS	LVDS	LVDS_U1	LVDS_U1_N
LVDS_DATA	LVDS	LVDS	LVDS_U2	LVDS_U2_P
	LVDS	LVDS	LVDS_U2	LVDS_U2_N
LVDS_CLK_UPPER	LVDS	LVDS	LVDS_UCLK	CLKLVDS_U_P
	LVDS	LVDS	LVDS_UCLK	CLKLVDS_U_N
LVDS_DATA	LVDS	LVDS	LVDS_L0	LVDS_L0_P
	LVDS	LVDS	LVDS_L0	LVDS_L0_N
LVDS_DATA	LVDS	LVDS	LVDS_L1	LVDS_L1_P
	LVDS	LVDS	LVDS_L1	LVDS_L1_N
LVDS_DATA	LVDS	LVDS	LVDS_L2	LVDS_L2_P
	LVDS	LVDS	LVDS_L2	LVDS_L2_N
LVDS_CLK_LOWER	LVDS	LVDS	LVDS_LCLK	CLKLVDS_L_P
	LVDS	LVDS	LVDS_LCLK	CLKLVDS_L_N
	VGA	VGA		GPU_VGA_R
	VGA	VGA		GPU_VGA_G
	VGA	VGA		GPU_VGA_B
	VGA_CONN	VGA_CONN		VGA_R
	VGA_CONN	VGA_CONN		VGA_G
	VGA_CONN	VGA_CONN		VGA_B
	TV	TV		GPU_TV_Y
	TV	TV		GPU_TV_C
	TV	TV		GPU_TV_COMP
	TV_CONN	TV_CONN		TV_Y
	TV_CONN	TV_CONN		TV_C
	TV_CONN	TV_CONN		TV_COMP

GPU (M11) DVI/DAC Outputs

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
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Page Notes

Power aliases required by this page:
- =PP3V3_RUN_SI - =PP1V5R3V3_DVO_VREF

Signal aliases required by this page:
- =SI_TMDS_RESET_L - =RP67xxPy (pinswappable series R)
- =SI_I2C_CLK
- =SI_I2C_DATA

BOM options provided by this page:
- TMDS_EXT - DVO_1V5 - DVO_3V3
- TMDS_DUAL - DVO_1V8

Net Spacing Type: TMDS

Net Physical Type: TMDS

NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
P300 GPU_DVO_LOWER	DVO	DVO		GPU_DVOD<0..11>	6 54
P307 GPU_DVO_BOTH	DVO	DVO		GPU_DVO_HSYNC	6 54 55
P312 GPU_DVO_BOTH	DVO	DVO		GPU_DVO_VSYNC	6 54 55
P311 GPU_DVO_BOTH	DVO	DVO		GPU_DVO_DE	6 54 55
P310 GPU_DVO_CLKP	DVO	DVO		GPU_DVO_CLKP	6 54 55
P313 TMDS_CLK	TMDS	TMDS	SI_TMDS_CLK	SI_TMDS_CLKP	54
P317	TMDS	TMDS	SI_TMDS_CLK	SI_TMDS_CLKN	54
P319 TMDS_DATA	TMDS	TMDS	SI_TMDS_D0	SI_TMDS_DP<0>	54
P318	TMDS	TMDS	SI_TMDS_D0	SI_TMDS_DN<0>	54
P327 TMDS_DATA	TMDS	TMDS	SI_TMDS_D1	SI_TMDS_DP<1>	54
P326	TMDS	TMDS	SI_TMDS_D1	SI_TMDS_DN<1>	54
P325 TMDS_DATA	TMDS	TMDS	SI_TMDS_D2	SI_TMDS_DP<2>	2 54
P324	TMDS	TMDS	SI_TMDS_D2	SI_TMDS_DN<2>	54

SILICON IMAGE TMDS

TMDS_EXT&TMDS_DUAL RP6707 10 (5% 1/16W SM-LF): 54 SI_TMDS_CLKN — TMDS_CLKN 54 57
TMDS_EXT&TMDS_DUAL RP6707 10 (5% 1/16W SM-LF): 54 SI_TMDS_CLKP — TMDS_CLKP 54 57
TMDS_EXT&TMDS_DUAL RP6708 10 (5% 1/16W SM-LF): 54 SI_TMDS_DN<0> — TMDS_DN<0> 54 57
TMDS_EXT&TMDS_DUAL RP6708 10 (5% 1/16W SM-LF): 54 SI_TMDS_DP<0> — TMDS_DP<0> 54 57
TMDS_EXT&TMDS_DUAL RP6709 10 (5% 1/16W SM-LF): 54 SI_TMDS_DN<1> — TMDS_DN<1> 54 57
TMDS_EXT&TMDS_DUAL RP6709 10 (5% 1/16W SM-LF): 54 SI_TMDS_DP<1> — TMDS_DP<1> 54 57
TMDS_EXT&TMDS_DUAL RP6710 10 (5% 1/16W SM-LF): 54 SI_TMDS_DN<2> — TMDS_DN<2> 54 57
TMDS_EXT&TMDS_DUAL RP6710 10 (5% 1/16W SM-LF): 54 2 SI_TMDS_DP<2> — TMDS_DP<2> 54 57

EXTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN

EXT_TMDS_CLK_CMF
TMDS_EXT&TMDS_DUAL R6760 49.9 (1% 1/16W MF-LF 402): 57 54 TMDS_CLKP
TMDS_EXT&TMDS_DUAL R6761 49.9 (1% 1/16W MF-LF 402): TMDS_CLKN 54 57
TMDS_EXT&TMDS_DUAL C6760 0.001uF (10% 50V CERM 402)

EXT_TMDS_D0_CMF
TMDS_EXT&TMDS_DUAL R6762 49.9 (1% 1/16W MF-LF 402): 57 54 TMDS_DP<0>
TMDS_EXT&TMDS_DUAL R6763 49.9 (1% 1/16W MF-LF 402): TMDS_DN<0> 54 57
TMDS_EXT&TMDS_DUAL C6762 0.001uF (10% 50V CERM 402)

EXT_TMDS_D1_CMF
TMDS_EXT&TMDS_DUAL R6764 49.9 (1% 1/16W MF-LF 402): 57 54 TMDS_DP<1>
TMDS_EXT&TMDS_DUAL R6765 49.9 (1% 1/16W MF-LF 402): TMDS_DN<1> 54 57
TMDS_EXT&TMDS_DUAL C6764 0.001uF (10% 50V CERM 402)

EXT_TMDS_D2_CMF
TMDS_EXT&TMDS_DUAL R6766 49.9 (1% 1/16W MF-LF 402): 57 54 TMDS_DP<2>
TMDS_EXT&TMDS_DUAL R6767 49.9 (1% 1/16W MF-LF 402): TMDS_DN<2> 54 57
TMDS_EXT&TMDS_DUAL C6766 0.001uF (10% 50V CERM 402)

TMDS_EXT&TMDS_DUAL L6723 180-OHM-1.5A (0603): =PP3V3_RUN_SI 10 54 55
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.38 mm
VOLTAGE=3.3V
PP3V3_SI_M_AVCC
TMDS_EXT&TMDS_DUAL C6723 10UF (10% 6.3V X5R 805)
TMDS_EXT&TMDS_DUAL C6724 100pF (5% 50V CERM 402)
TMDS_EXT&TMDS_DUAL C6725 100pF (5% 50V CERM 402)

TMDS_EXT&TMDS_DUAL L6720 180-OHM-1.5A (0603): =PP3V3_RUN_SI 10 54 55
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.38 mm
VOLTAGE=3.3V
PP3V3_SI_M_VCC
C6720 10UF (10% 6.3V X5R 805)
TMDS_EXT&TMDS_DUAL C6721 100pF (5% 50V CERM 402)
TMDS_EXT&TMDS_DUAL C6722 100pF (5% 50V CERM 402)
TMDS_EXT&TMDS_DUAL

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.38 mm
PP3V3_SI_M_PVCC

TMDS_EXT&TMDS_DUAL L6726 180-OHM-1.5A (0603): =PP3V3_RUN_SI 10 54 55
TMDS_EXT&TMDS_DUAL C6726 10UF (10% 6.3V X5R 805)
TMDS_EXT&TMDS_DUAL C6727 100pF (5% 50V CERM 402)
TMDS_EXT&TMDS_DUAL C6728 10UF (10% 6.3V X5R 805)
TMDS_EXT&TMDS_DUAL C6729 100pF (5% 50V CERM 402)

Place C6726/C6727 at pin 28
Place C6728/C6729 at pin 46

TMDS_EXT&TMDS_DUAL R6734 10K (5% 1/16W MF-LF 402)
TMDS_EXT&TMDS_DUAL R6752 301 (1% 1/16W MF-LF 402)
NO STUFF R6754 4.99K (1% 1/16W MF-LF 402)

Lower DVO Termination

Place close to GPU

One each for: GPU_DVOD<0..11>, GPU_DVO_HSYNC, GPU_DVO_VSYNC, GPU_DVO_DE, GPU_DVO_CLKP

TMDS_EXT&TMDS_DUAL RP6720 10 (5% 1/16W SM-LF): 6 =RP6720P1 — =RP6720P8 6
TMDS_EXT&TMDS_DUAL RP6720 10: 6 =RP6720P2 — =RP6720P7 6
TMDS_EXT&TMDS_DUAL RP6720 10: 6 =RP6720P3 — =RP6720P6 6
TMDS_EXT&TMDS_DUAL RP6720 10: 6 =RP6720P4 — =RP6720P5 6
TMDS_EXT&TMDS_DUAL RP6721 10: 6 =RP6721P1 — =RP6721P8 6
TMDS_EXT&TMDS_DUAL RP6721 10: 6 =RP6721P2 — =RP6721P7 6
TMDS_EXT&TMDS_DUAL RP6721 10: 6 =RP6721P3 — =RP6721P6 6
TMDS_EXT&TMDS_DUAL RP6721 10: 6 =RP6721P4 — =RP6721P5 6
TMDS_EXT&TMDS_DUAL RP6722 10: 6 =RP6722P1 — =RP6722P8 6
TMDS_EXT&TMDS_DUAL RP6722 10: 6 =RP6722P2 — =RP6722P7 6
TMDS_EXT&TMDS_DUAL RP6722 10: 6 =RP6722P3 — =RP6722P6 6
TMDS_EXT&TMDS_DUAL RP6722 10: 6 =RP6722P4 — =RP6722P5 6
TMDS_EXT&TMDS_DUAL RP6723 10: 6 =RP6723P1 — =RP6723P8 6
TMDS_EXT&TMDS_DUAL RP6723 10: 6 =RP6723P2 — =RP6723P7 6
TMDS_EXT&TMDS_DUAL RP6723 10: 6 =RP6723P3 — =RP6723P6 6
TMDS_EXT&TMDS_DUAL RP6723 10: 6 =RP6723P4 — =RP6723P5 6

CRITICAL U6700 SIL1178CS48 TSSOP

Pin	Signal	Pin	Signal
27	SCL	33	TXC+
26	SDA	32	TXC-
24	CTL3/A1	36	TX0+
25	RST*	35	TX0-
47	SYNCO/SYNCI	39	TX1+
44	EHTPLG	38	TX1-
18	D0	42	TX2+
17	D1	41	TX2-
16	D2	30	EXT_SWING
15	D3	2	VREF
14	D4	48	MSEN
13	D5		
10	D6		
9	D7		
8	D8		
7	D9		
6	D10		
5	D11		
19	DE		
20	HSYNC		
21	VSYNC		
12	IDCK+		
11	IDCK-		

Power pins: PVCC1 28, PVCC2 46, AVCC 40, AVCC 34, AVCC 22, VCC 23, VCC 3
Ground pins: PGND 29, PGND 45, AGND 31, AGND 43, AGND 37, GND 1, GND 23, GND 4, THRML PAD 49

8 =I2C_SI_M_SCL
8 =I2C_SI_M_SDA
SI_M_A1
55 11 =SI_TMDS_RESET_L
55 SI_SYNC
55 SI_HTPLG
54 6 GPU_DVOD<0>
54 6 GPU_DVOD<1>
54 6 GPU_DVOD<2>
54 6 GPU_DVOD<3>
54 6 GPU_DVOD<4>
54 6 GPU_DVOD<5>
54 6 GPU_DVOD<6>
54 6 GPU_DVOD<7>
54 6 GPU_DVOD<8>
54 6 GPU_DVOD<9>
54 6 GPU_DVOD<10>
54 6 GPU_DVOD<11>
55 54 6 GPU_DVO_DE
55 54 6 GPU_DVO_HSYNC
55 54 6 GPU_DVO_VSYNC
55 54 6 GPU_DVO_CLKP
55 54 SI_IDCK_N
SI_M_MSEN
SI_TMDS_CLKP 54
SI_TMDS_CLKN 54
SI_TMDS_DP<0> 54
SI_TMDS_DN<0> 54
SI_TMDS_DP<1> 54
SI_TMDS_DN<1> 54
SI_TMDS_DP<2> 2 54
SI_TMDS_DN<2> 54
SI_M_EXTSWING
SI_VREF 54 55

TMDS_EXT&TMDS_DUAL R6730 10K (5% 1/16W MF-LF 402)
NO STUFF R6732 100K (5% 1/16W MF-LF 402)
DVO_3V3 R6733 1K (5% 1/16W MF-LF 402)
TMDS_EXT&TMDS_DUAL R6731 10K (5% 1/16W MF-LF 402)

The DVO bus can be run with 3.3V or 1.5V/1.8V signaling. The power rail for the reference should be connected to the GPU DVO rail.

=PP1V5R3V3_DVO_VREF 47
TMDS_EXT&TMDS_DUAL R6740 1K (1% 1/16W MF-LF 402)
DVO_1V5&DVO_1V8 R6741 1K (1% 1/16W MF-LF 402)
DVO_1V5&DVO_1V8 R6742 0 (5% 1/16W MF-LF 402): 55 54 SI_IDCK_N
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
TMDS_EXT&TMDS_DUAL C6740 0.1uF (20% 10V CERM 402)

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
P316	TMDS	TMDS	TMDS_CLK	TMDS_CLKP	54 57
P330	TMDS	TMDS	TMDS_CLK	TMDS_CLKN	54 57
P331	TMDS	TMDS	TMDS_D0	TMDS_DP<0>	54 57
P332	TMDS	TMDS	TMDS_D0	TMDS_DN<0>	54 57
P333	TMDS	TMDS	TMDS_D1	TMDS_DP<1>	54 57
P334	TMDS	TMDS	TMDS_D1	TMDS_DN<1>	54 57
P335	TMDS	TMDS	TMDS_D2	TMDS_DP<2>	54 57
P336	TMDS	TMDS	TMDS_D2	TMDS_DN<2>	54 57

Lower TMDS Transmitter

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 67 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_RUN_SI

Signal aliases required by this page:
- =SI_I2C_CLK
- =SI_I2C_DATA
- =SI_TMDS_RESET_L
- =RP68xxPy (pinswappable series R)

BOM options provided by this page:
- TMDS_DUAL

Net Spacing Type: TMDS

Net Physical Type: TMDS

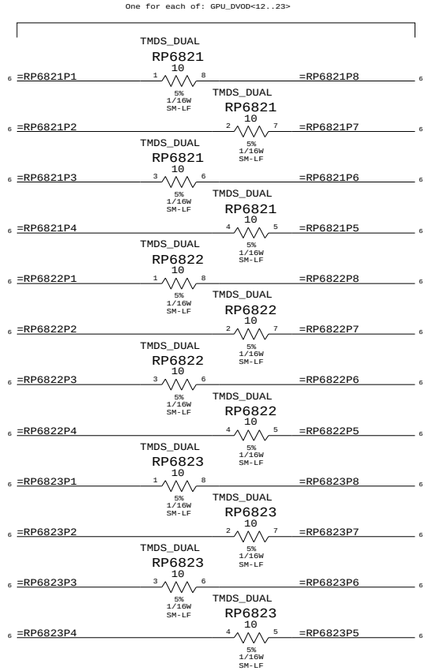
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

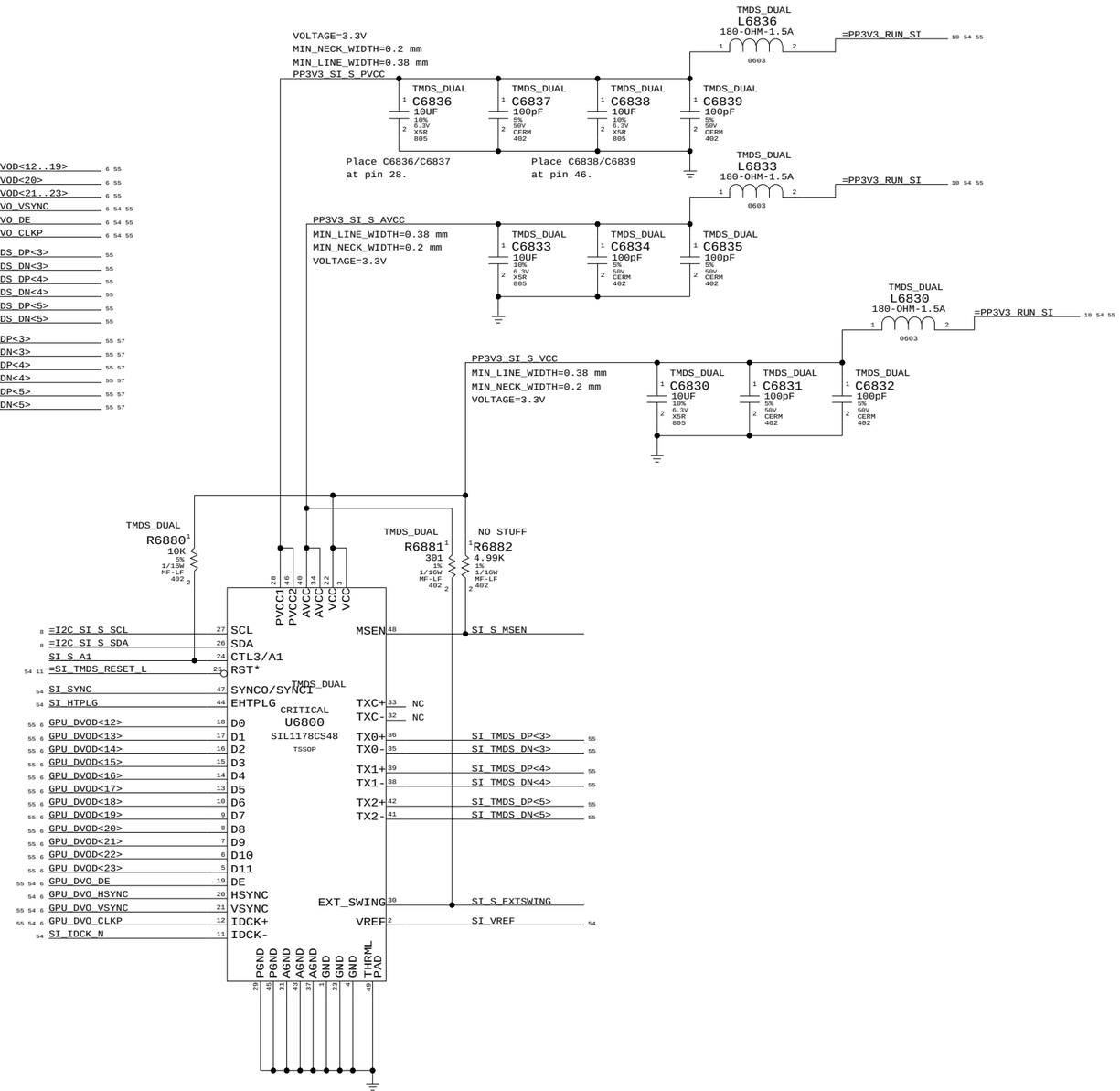
	ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
154	GPU_DVO_UPPER	DVO	DVO		GPU_DVOD<12..19>	6 55
155	GPU_DVOD20	DVO	DVO		GPU_DVOD<20>	6 55
156	GPU_DVO_UPPER	DVO	DVO		GPU_DVOD<21..23>	6 55
157		PROVIDED BY LOWER TXMR			GPU_DVO_VSYNC	6 54 55
158		PROVIDED BY LOWER TXMR			GPU_DVO_DE	6 54 55
159		PROVIDED BY LOWER TXMR			GPU_DVO_CLKP	6 54 55
160						
174	TMDS_DATA	TMDS	TMDS	SI_TMDS_D3	SI_TMDS_DP<3>	55
175		TMDS	TMDS	SI_TMDS_D3	SI_TMDS_DN<3>	55
176	TMDS_DATA	TMDS	TMDS	SI_TMDS_D4	SI_TMDS_DP<4>	55
177		TMDS	TMDS	SI_TMDS_D4	SI_TMDS_DN<4>	55
178	TMDS_DATA	TMDS	TMDS	SI_TMDS_D5	SI_TMDS_DP<5>	55
179		TMDS	TMDS	SI_TMDS_D5	SI_TMDS_DN<5>	55
180		TMDS	TMDS	TMDS_D3	TMDS_DP<3>	55 57
181		TMDS	TMDS	TMDS_D3	TMDS_DN<3>	55 57
182		TMDS	TMDS	TMDS_D4	TMDS_DP<4>	55 57
183		TMDS	TMDS	TMDS_D4	TMDS_DN<4>	55 57
184		TMDS	TMDS	TMDS_D5	TMDS_DP<5>	55 57
185		TMDS	TMDS	TMDS_D5	TMDS_DN<5>	55 57

Upper DVO series termination

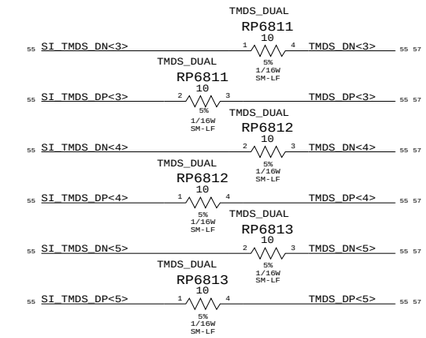
Place close to GPU

One for each of: GPU_DVOD<12..23>

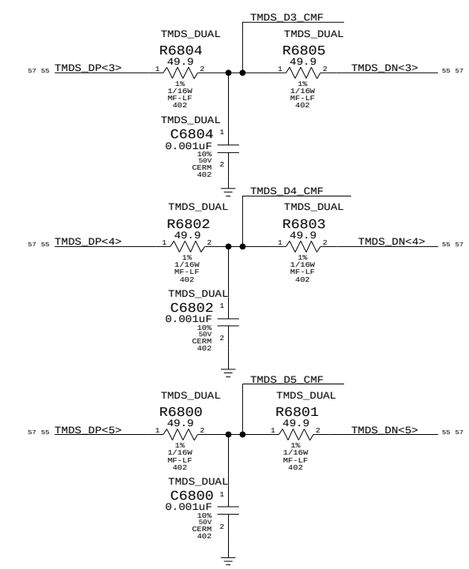




Upper Channel Series Termination



Upper Channel Common-mode Termination



Upper TMDS Transmitter

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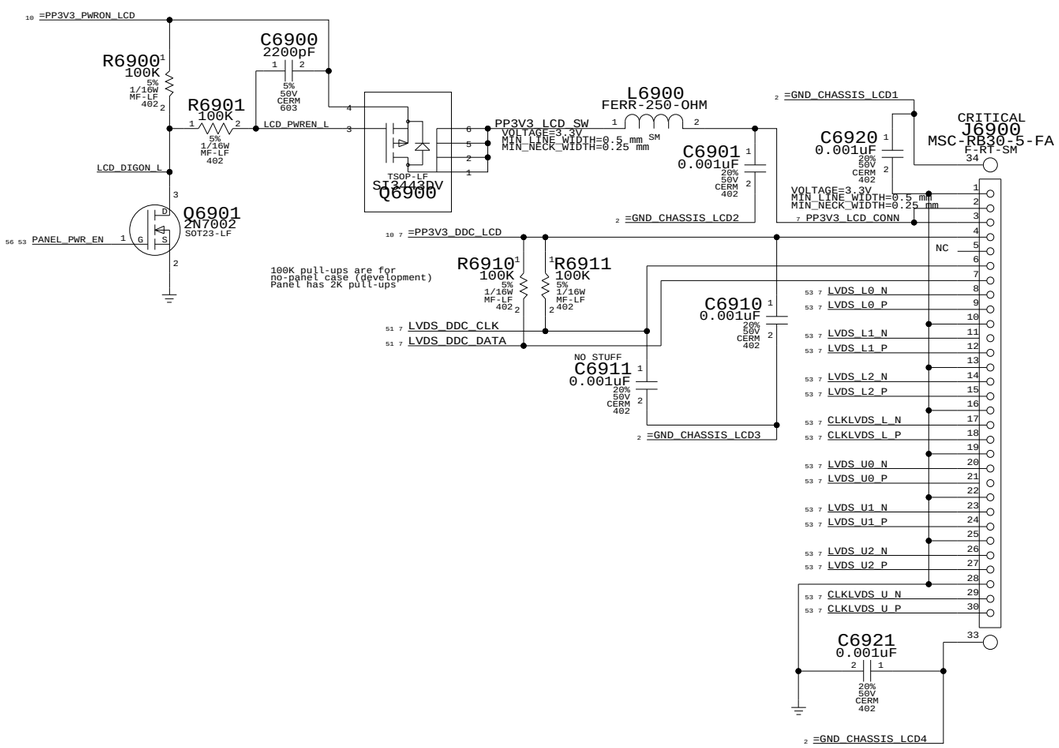
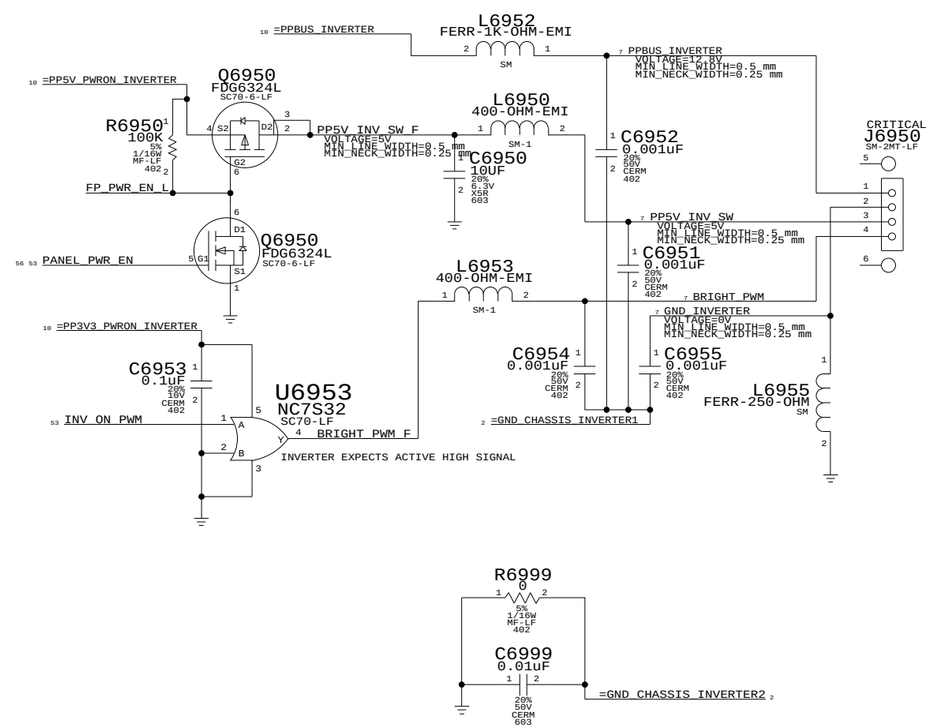
D	051-6839	E
SCALE NONE	SHT 68 OF 115	

LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Conns

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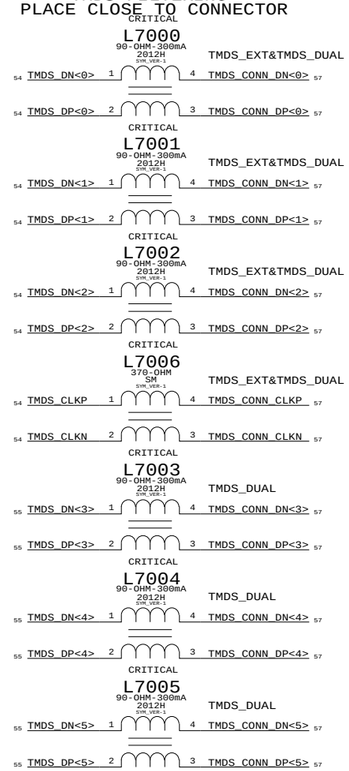
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 69 OF 115	

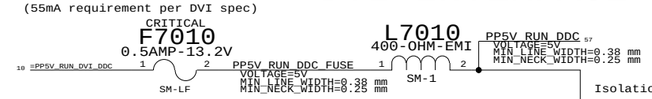
DVI INTERFACE

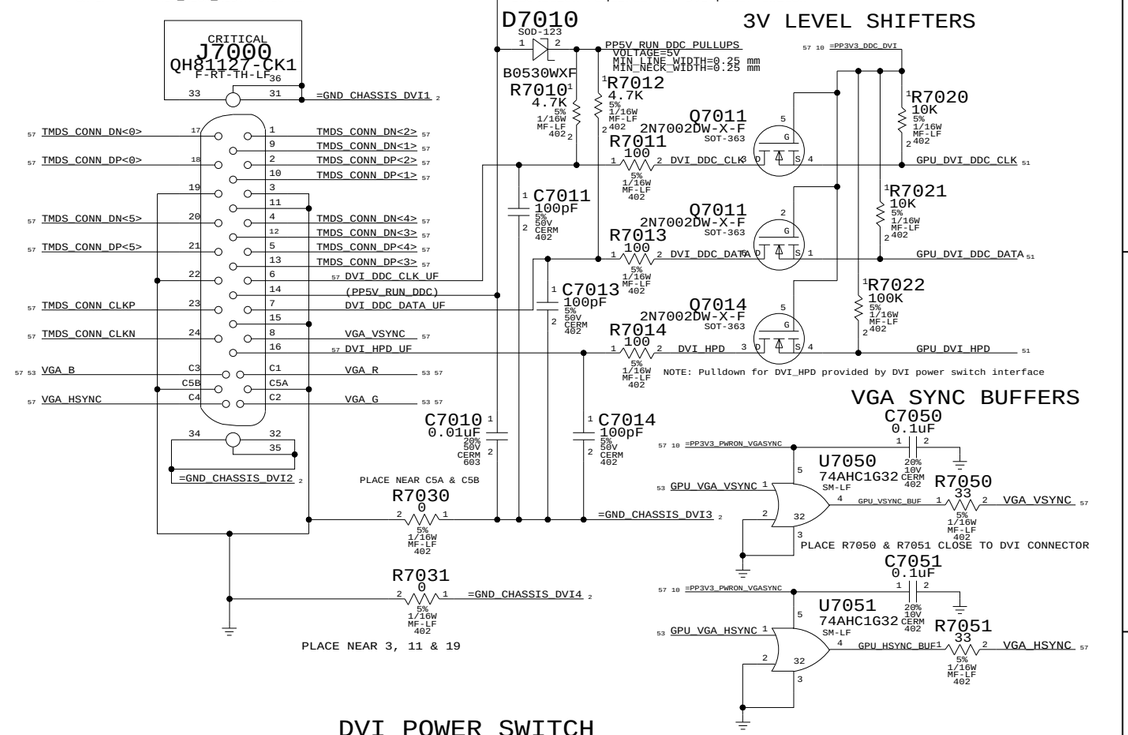
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
1540	TMDS_CONN	TMDS_CONN	TMDS_CONN_CLK	TMDS_CONN_CLKP
1540	TMDS_CONN	TMDS_CONN	TMDS_CONN_CLK	TMDS_CONN_CLKN
1600	TMDS_CONN	TMDS_CONN	TMDS_CONN_D0	TMDS_CONN_DP<0>
1601	TMDS_CONN	TMDS_CONN	TMDS_CONN_D0	TMDS_CONN_DN<0>
1602	TMDS_CONN	TMDS_CONN	TMDS_CONN_D1	TMDS_CONN_DP<1>
1603	TMDS_CONN	TMDS_CONN	TMDS_CONN_D1	TMDS_CONN_DN<1>
1604	TMDS_CONN	TMDS_CONN	TMDS_CONN_D2	TMDS_CONN_DP<2>
1605	TMDS_CONN	TMDS_CONN	TMDS_CONN_D2	TMDS_CONN_DN<2>
1606	TMDS_CONN	TMDS_CONN	TMDS_CONN_D3	TMDS_CONN_DP<3>
1607	TMDS_CONN	TMDS_CONN	TMDS_CONN_D3	TMDS_CONN_DN<3>
1608	TMDS_CONN	TMDS_CONN	TMDS_CONN_D4	TMDS_CONN_DP<4>
1609	TMDS_CONN	TMDS_CONN	TMDS_CONN_D4	TMDS_CONN_DN<4>
1610	TMDS_CONN	TMDS_CONN	TMDS_CONN_D5	TMDS_CONN_DP<5>
1611	TMDS_CONN	TMDS_CONN	TMDS_CONN_D5	TMDS_CONN_DN<5>

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

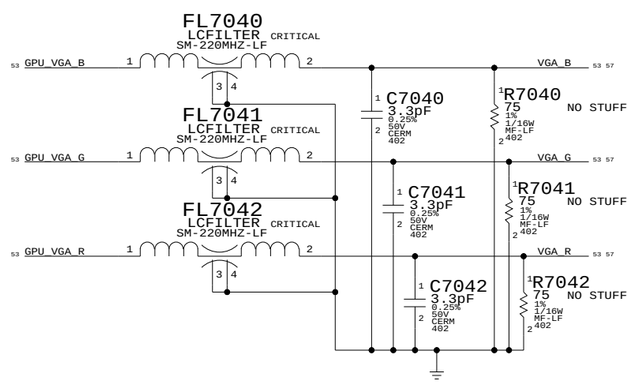


DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



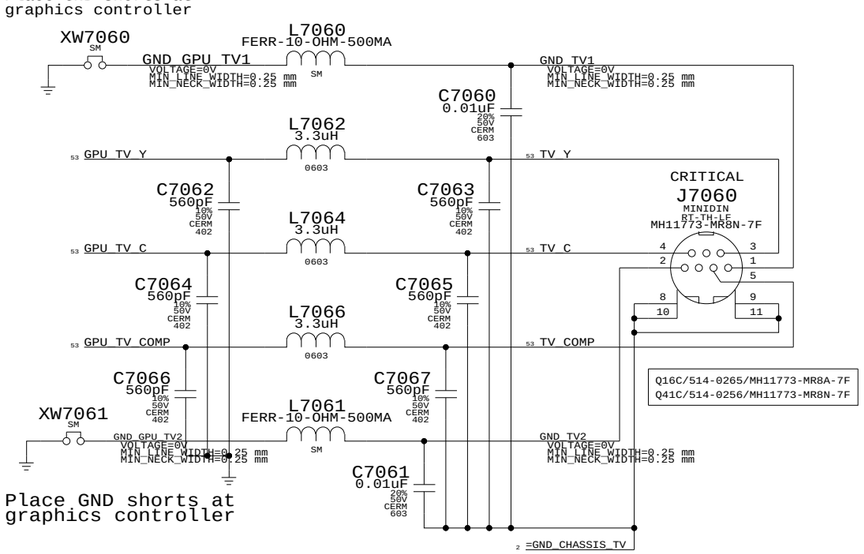


ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

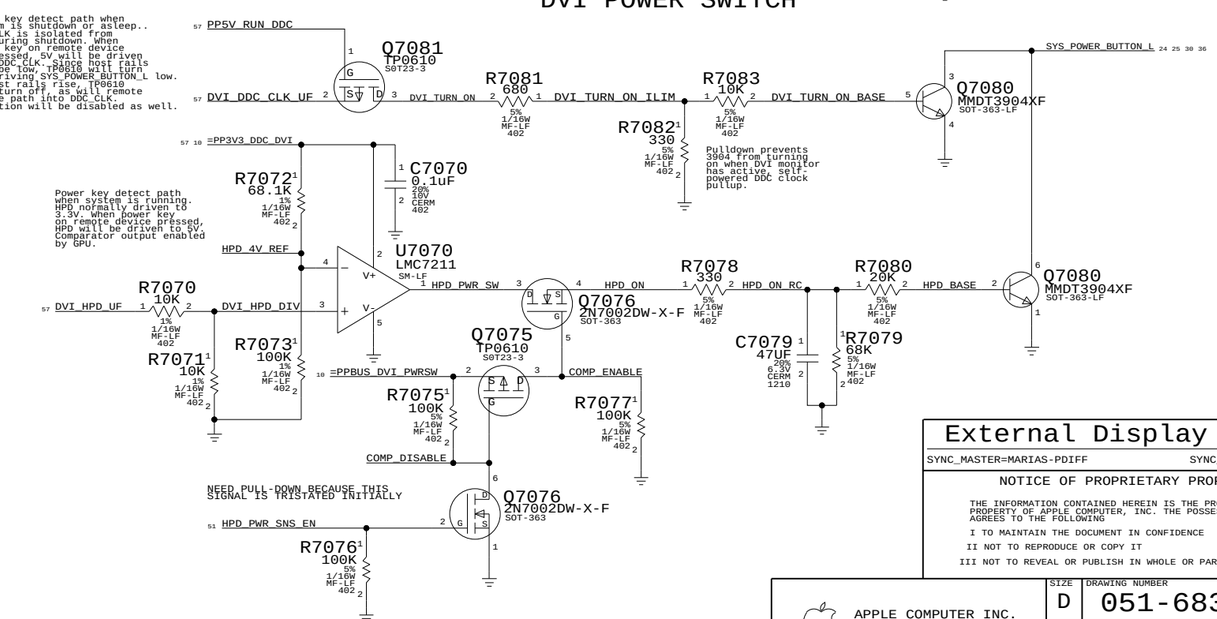


Place GND shorts at graphics controller

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from GPU during shutdown. When power key on remote device is pressed, 5V will be driven into DDC CLK. Since host rails will be low, TP0610 will turn on, driving SYS_POWER_BUTTON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. Comparator output enabled by GPU.



External Display Conns

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 70 OF 115	

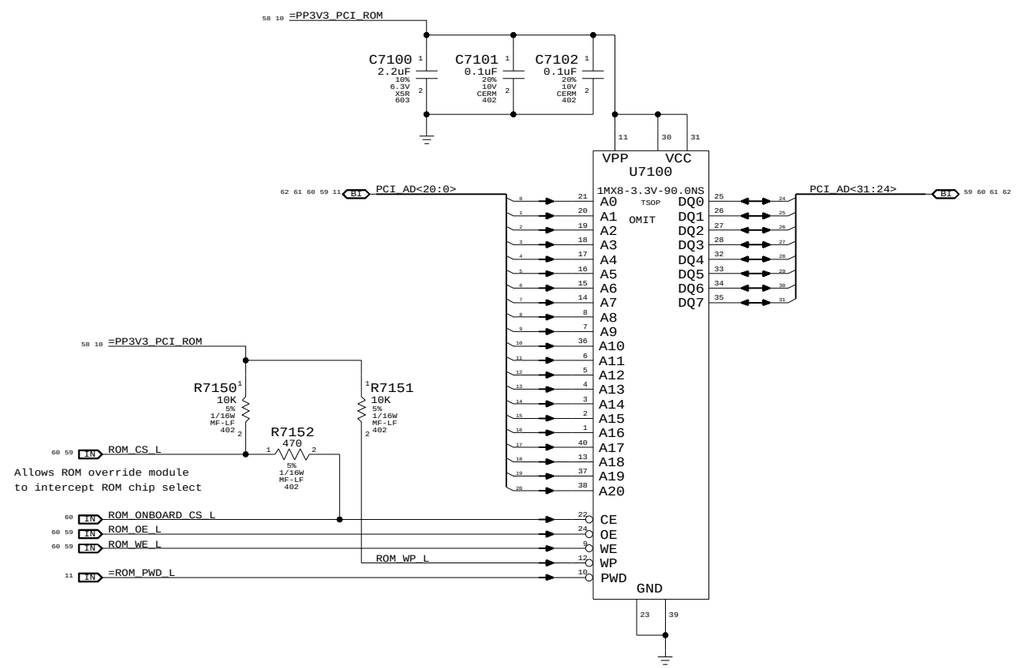
Page Notes

Power aliases required by this page:
- =PP3V3_PCI_ROM

Signal aliases required by this page:
- =ROM_PWD_L

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7100 part number.



BootROM

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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D	051-6839	E
SCALE NONE	SHT 71 OF 115	

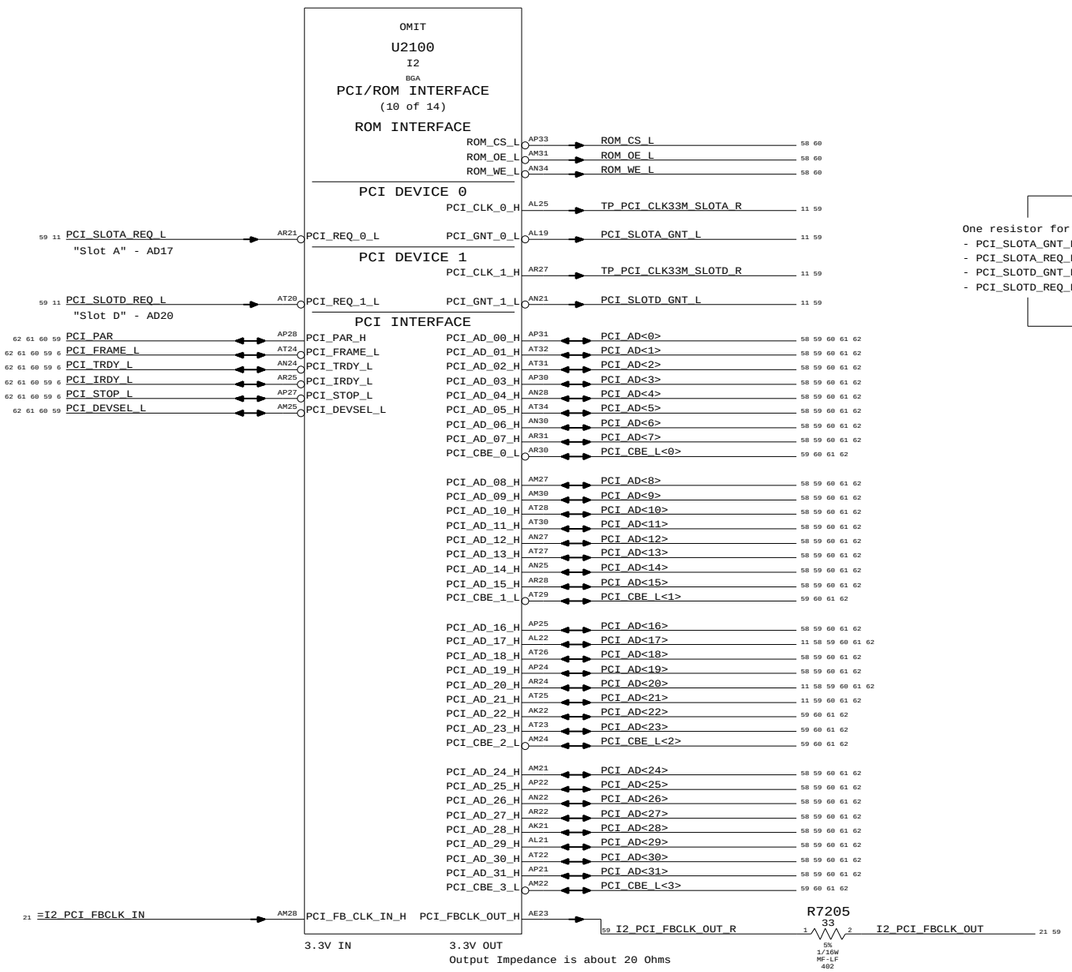
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
PCI_CLK_SLOTA	CLOCK	CLOCK		TP_PCI_CLK33M_SLOTA_R	11 59
PCI_CLK_SLOTD	CLOCK	CLOCK		TP_PCI_CLK33M_SLOTD_R	11 59
I2_PCI_FBCLK	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_OUT_R	59
	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_OUT	21 59
PCI_AD16_0	PCI	PCI		PCI_AD<16..0>	58 59 60 61 62 (BOOTROM ADDR)
PCI_AD17	PCI	PCI		PCI_AD<17>	11 58 59 60 61 62 (BOOTROM ADDR/SLOT A IDSEL)
PCI_AD19_18	PCI	PCI		PCI_AD<19..18>	58 59 60 61 62 (BOOTROM ADDR)
PCI_AD20	PCI	PCI		PCI_AD<20>	11 58 59 60 61 62 (SLOT D IDSEL)
PCI_AD21	PCI	PCI		PCI_AD<21>	11 59 60 61 62 (SLOT E IDSEL)
PCI_AD23_22	PCI	PCI		PCI_AD<23..22>	59 60 61 62 (PCI ONLY)
PCI_AD31_24	PCI	PCI		PCI_AD<31..24>	58 59 60 61 62 (BOOTROM DATA)
PCI_CBE	PCI	PCI		PCI_CBE_L<3..0>	59 60 61 62
PCI_CTL	PCI	PCI		PCI_FRAME_L	6 59 60 61 62
PCI_CTL	PCI	PCI		PCI_DEVSEL_L	59 60 61 62
PCI_CTL	PCI	PCI		PCI_IRDY_L	6 59 60 61 62
PCI_CTL	PCI	PCI		PCI_TRDY_L	6 59 60 61 62
PCI_CTL	PCI	PCI		PCI_STOP_L	6 59 60 61 62
PCI_PAR	PCI	PCI		PCI_PAR	59 60 61 62
	PCI	PCI		PCI_SLOTA_REQ_L	11 59
	PCI	PCI		PCI_SLOTA_GNT_L	11 59
	PCI	PCI		PCI_SLOTD_REQ_L	11 59
	PCI	PCI		PCI_SLOTD_GNT_L	11 59

Page Notes

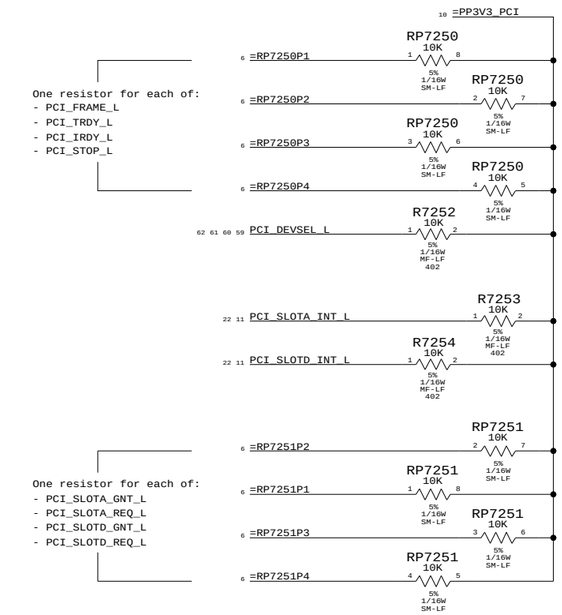
Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
- =I2_PCI_FBCLK_IN - PCI feedback clock input. Length should match that of longest clock from I2 to PCI device.

BOM options provided by this page:
(NONE)



PCI PULL-UPS



SLOT E REQ/GNT pull-ups
not provided by this page.

I2 PCI Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 72 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
	CLOCK	CLOCK	

PCI =PCI_CLK33M_AIRPORT 11 60

Page Notes

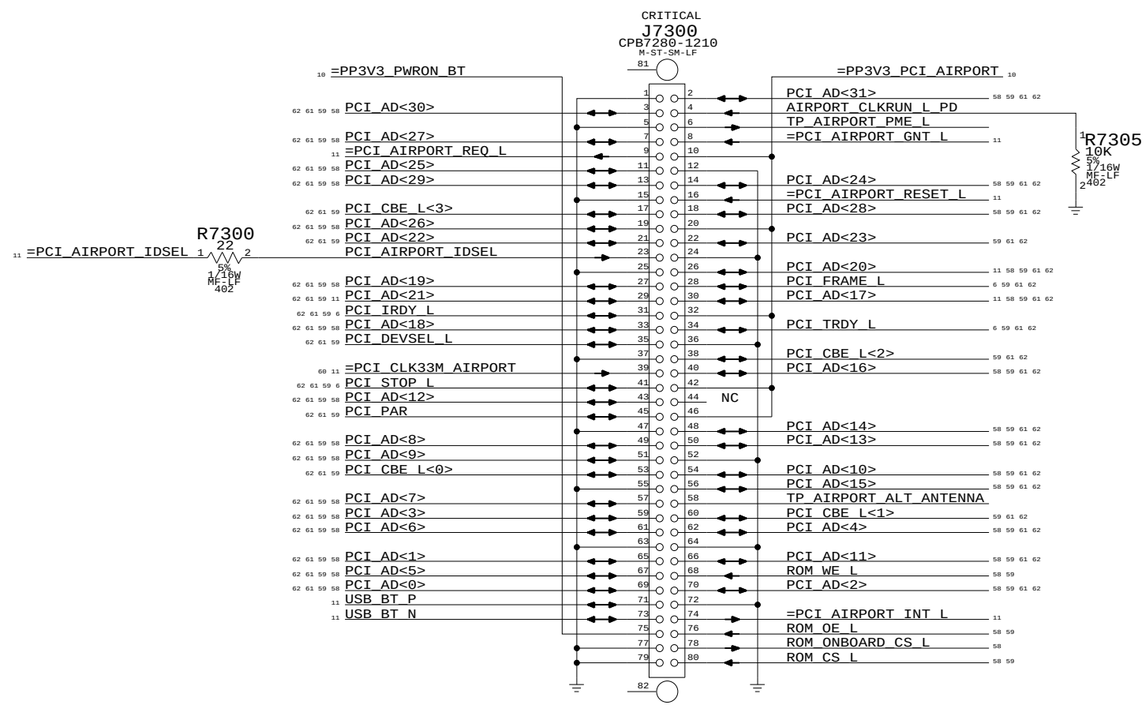
Power aliases required by this page:
- =PP3V3_PCI (802.11g Power)
- =PP3V3_PWRON_BT (Bluetooth Power)

Signal aliases required by this page:
- =PCI_CLK33M_AIRPORT (33MHz PCI clock)
- =PCI_AIRPORT_RESET_L (PCI Reset)
- =USB_BT_P (Bluetooth USB D+)
- =USB_BT_N (Bluetooth USB D-)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



Q85 Connector
Q16C/516S0361/F-ST-SM
Q41C/516S0352/M-ST-SM-LF

Q85 AIRPORT/BT CONN

SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 73 OF 115	

NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI2	CLOCK	CLOCK	

=PCI_CLK33M_CBUS

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON PPVCC_CBUS_SW

PCI1510 PULL-UPS

PC CARD/CARDBUS CONNECTOR

Cardbus

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 74 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
fo	CLOCK	CLOCK	

=PCI_CLK33M_USB2 11 62

Page Notes

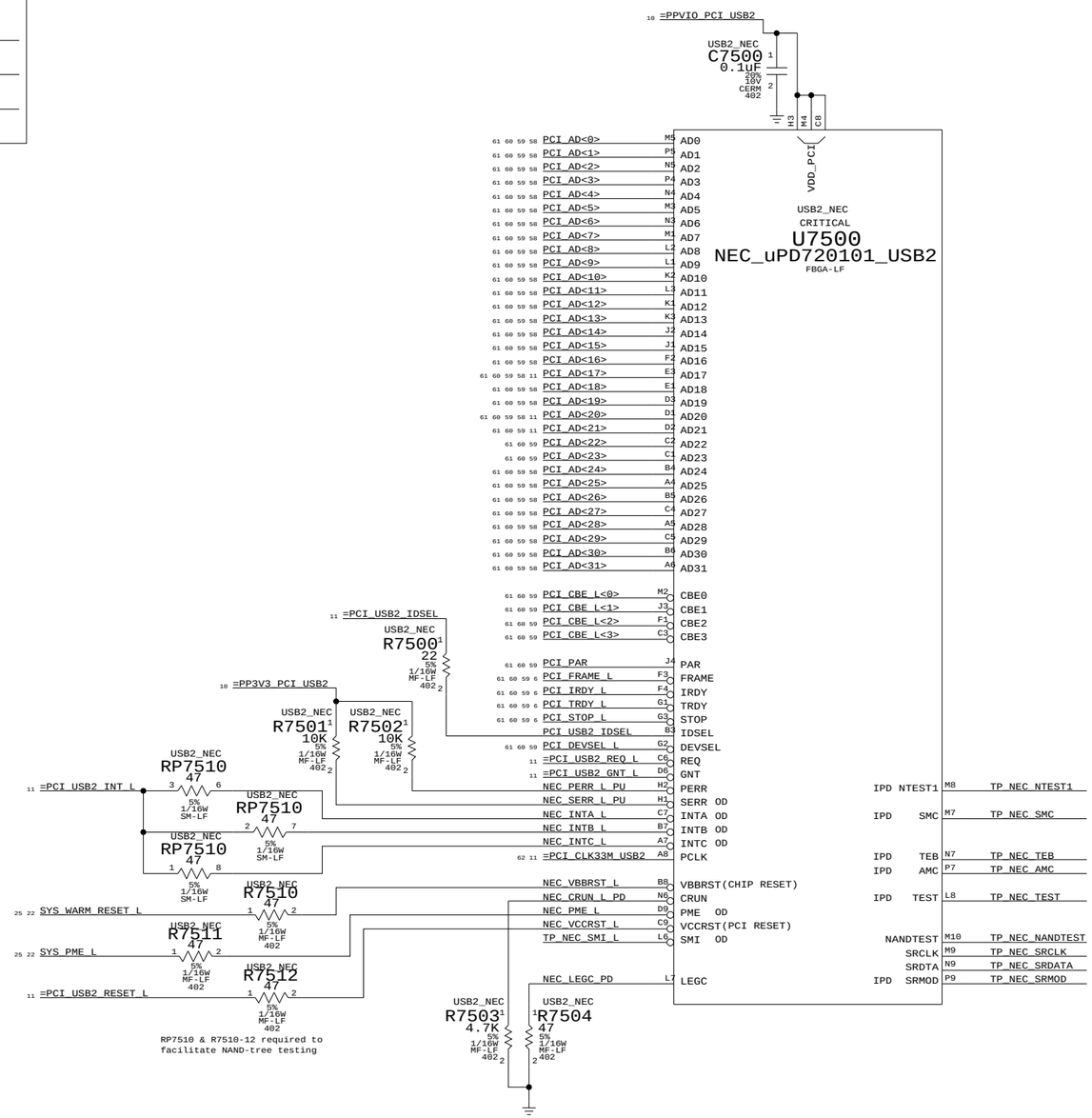
Power aliases required by this page:
- =PPVIO_PCI (to 3.3V or 5V)
- =PP3V3_PCI_USB2 (D3cold rail)

Signal aliases required by this page:
- =PCI_CLK33M_USB2
- =PCI_USB2_REQ_L - =PCI_USB2_IDSEL
- =PCI_USB2_GNT_L - =PCI_USB2_RESET_L
- =PCI_USB2_INT_L

BOM options provided by this page:
- USB2_NEC

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



NEC USB2

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 75 OF 115	

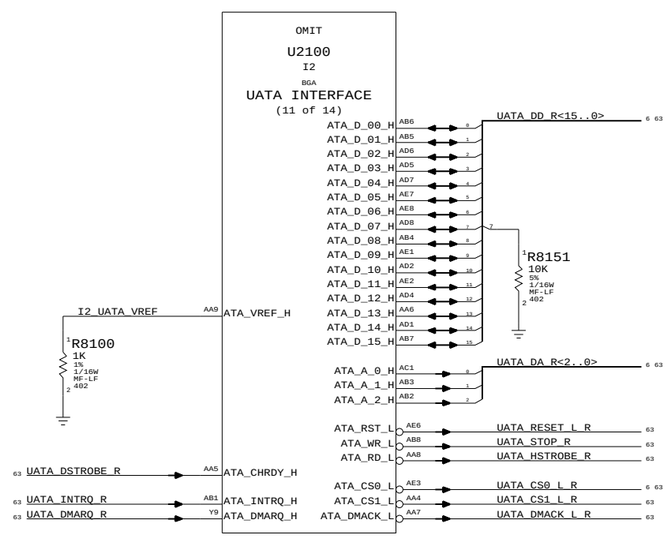
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
UATA_DD	UATA	UATA		UATA_DD_R<15..8>	6 63
UATA_DD7	UATA	UATA		UATA_DD_R<7>	6 63
UATA_DD	UATA	UATA		UATA_DD_R<6..0>	6 63
UATA_HOST	UATA	UATA		UATA_DA_R<2..0>	6 63
UATA_HOST	UATA	UATA		UATA_CS0_L_R	6 63
UATA_HOST	UATA	UATA		UATA_CS1_L_R	63
UATA_HSTROBE	UATA	UATA		UATA_HSTROBE_R	63
UATA_HOST	UATA	UATA		UATA_STOP_R	63
UATA_HOST_R	UATA	UATA		UATA_DMACK_L_R	63
UATA_HOST_R	UATA	UATA		UATA_RESET_L_R	63
UATA_DSTROBE	UATA	UATA		UATA_DSTROBE_R	63
UATA_DEV_R	UATA	UATA		UATA_DMARQ_R	63
UATA_DEV_R	UATA	UATA		UATA_INTRQ_R	63
	UATA	UATA		UATA_DD<15..0>	6 7 64
	UATA	UATA		UATA_DA<2..0>	6 7 64
	UATA	UATA		UATA_CS0_L	6 7 64
	UATA	UATA		UATA_CS1_L	7 63 64
	UATA	UATA		UATA_HSTROBE	7 63 64
	UATA	UATA		UATA_STOP	7 63 64
	UATA	UATA		UATA_DMACK_L	7 63 64
	UATA	UATA		UATA_RESET_L	7 63 64
	UATA	UATA		UATA_DSTROBE	7 63 64
	UATA	UATA		UATA_DMARQ	7 63 64
	UATA	UATA		UATA_INTRQ	7 63 64

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

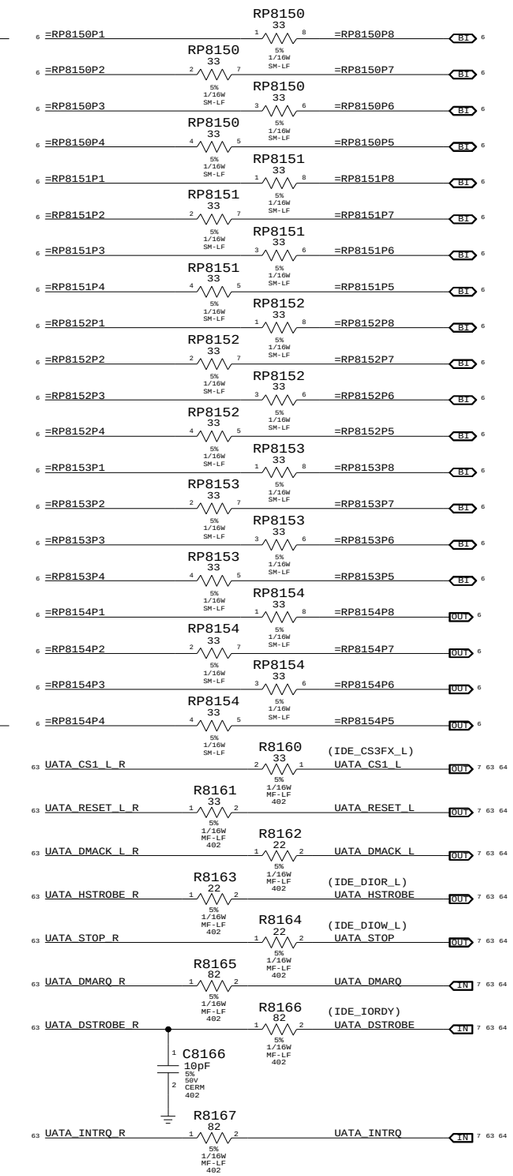
BOM options provided by this page:
(NONE)



UATA100 SERIES TERMINATION

PLACE CLOSE TO I2

One resistor for each of:
- UATA_DD<15..0>(_R)
- UATA_DA<2..0>(_R)
- UATA_CS0_L(_R)
(IDE_CS1FX_L)



I2 UATA Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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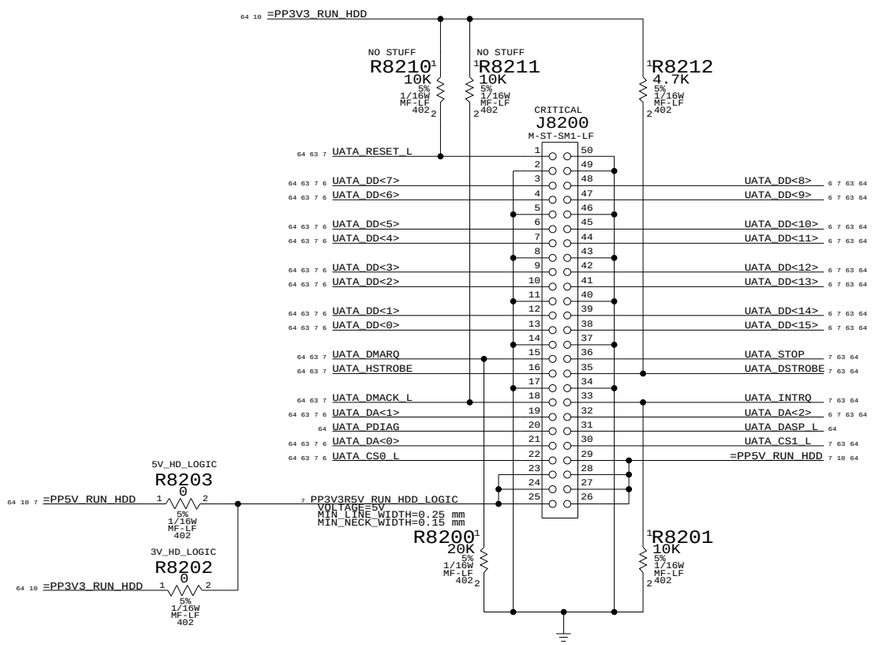
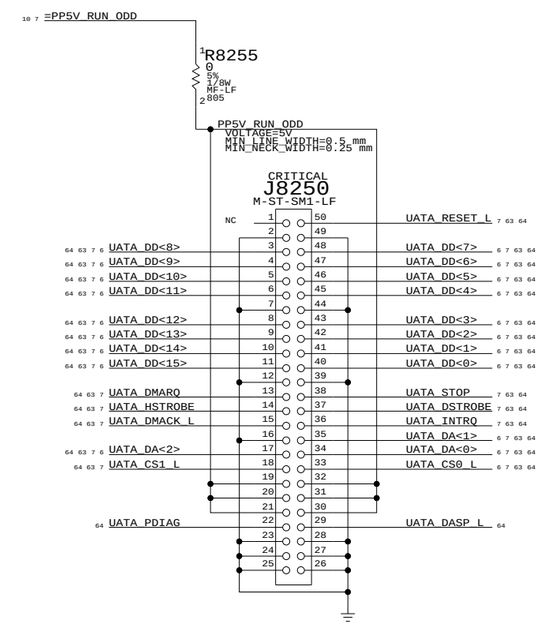
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 81 OF 115	

HDD CONNECTOR



ODD CONNECTOR



ATA Connectors

Q16C/516S0357/M-ST-SM2-LF
Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 82 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
ENET_RX_CLK25M	CLOCK	CLOCK		ENET_CLK25M_TX	11 65
ENET_RX_CLK125M	CLOCK	CLOCK		ENET_CLK125M_RX	11 65
ENET_GBE_REF	CLOCK	CLOCK		ENET_CLK125M_GBE_REF	11 65
ENET_TX_CLK	CLOCK	CLOCK		ENET_CLK125M_GTX_R	65 66
ENET_RXD3_0	ENET	ENET		ENET_RXD<3..0>	9 11 65
ENET_RXD7_4	ENET	ENET		ENET_RXD<7..4>	9 11 65
ENET_RX_DV	ENET	ENET		ENET_RX_DV	9 11 65
ENET_RX_CTL	ENET	ENET		ENET_RX_ER	9 11 65
ENET_TXD3_0	ENET	ENET		ENET_TXD_R<3..0>	11 65
ENET_TXD7_4	ENET	ENET		ENET_TXD_R<7..4>	11 65
ENET_TX_EN	ENET	ENET		ENET_TX_EN_R	11 65
ENET_TX_ER	ENET	ENET		ENET_TX_ER_R	11 65
ENET_COL	ENET	ENET		ENET_COL	9 11 65
ENET_RX_CTL	ENET	ENET		ENET_CRS	9 11 65
ENET_MDC	ENET	ENET		ENET_MDC	9 11 65
ENET_MDIO	ENET	ENET		ENET_MDIO	9 11 65
	ENET	ENET		I2_ENET_MDIO	65

Page Notes

Power aliases required by this page:
- =PP2V5R3V3_PWRON_I2_ENET

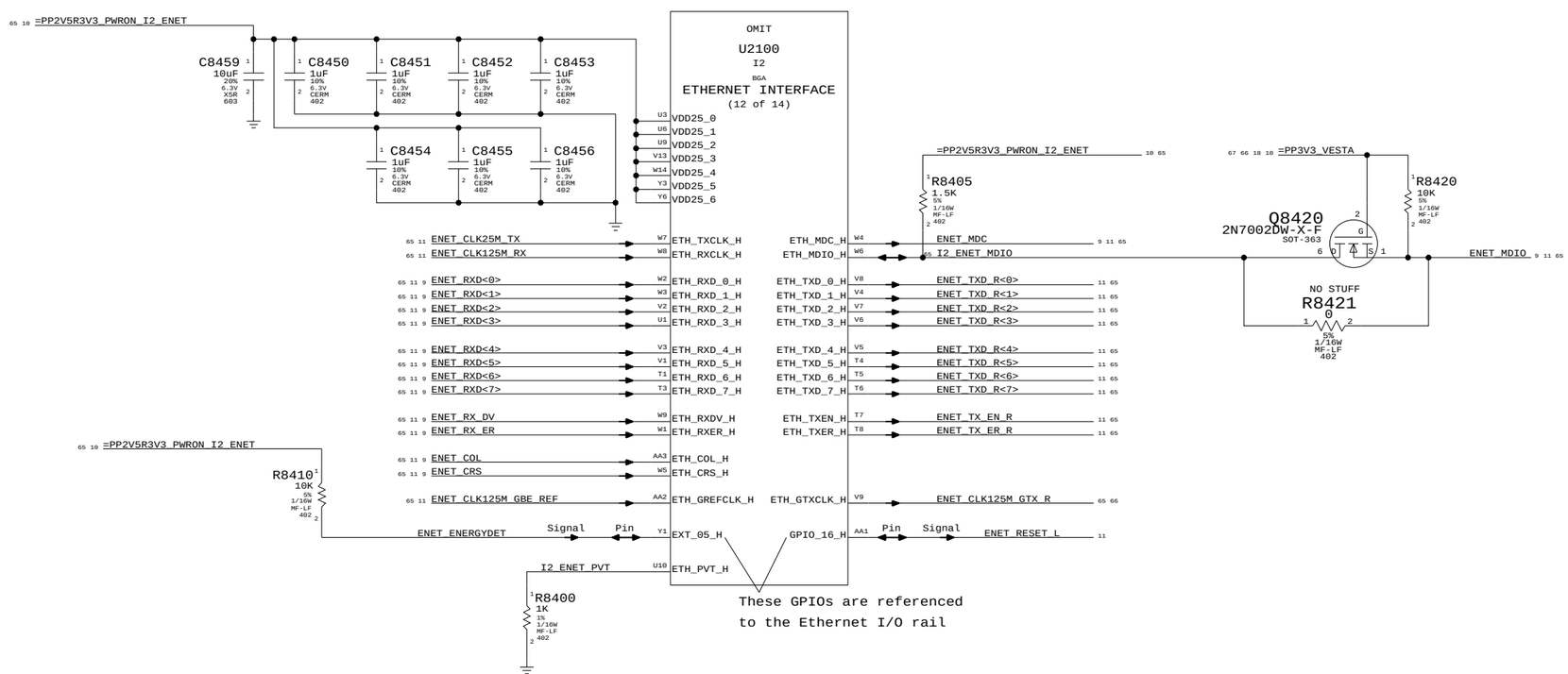
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not provide any series termination. Any termination, including clock signals, should be provided by the PHY page or a non-shared schematic page.

NOTE: All I2 GPIOs should have a pull-up or pull-down resistor. This page does not provide a resistor for GPIO 16. It must be provided by the PHY page or a non-shared schematic page.

NOTE: ENET_RX_DV has a hold spec violation on I2. May want to lengthen net by ~250ps. Net has a unique ECSet name to allow this.



I2 Ethernet Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 84 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK125M_GBE_REF_R 66
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK125M_RX_R 66
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK25M_TX_R 66
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	ENETCONN_0_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	ENETCONN_0_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	ENETCONN_1_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	ENETCONN_1_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	ENETCONN_2_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	ENETCONN_2_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	ENETCONN_3_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	ENETCONN_3_N 66 67
VESTA_CLK25M_XTAL	XTAL	XTAL		VESTA_CLK25M_XTALI 66
	XTAL	XTAL		VESTA_CLK25M_XTALO 66
	XTAL	XTAL		VESTA_CLK25M_XTALO_R 66

Page Notes

Power aliases required by this page:
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

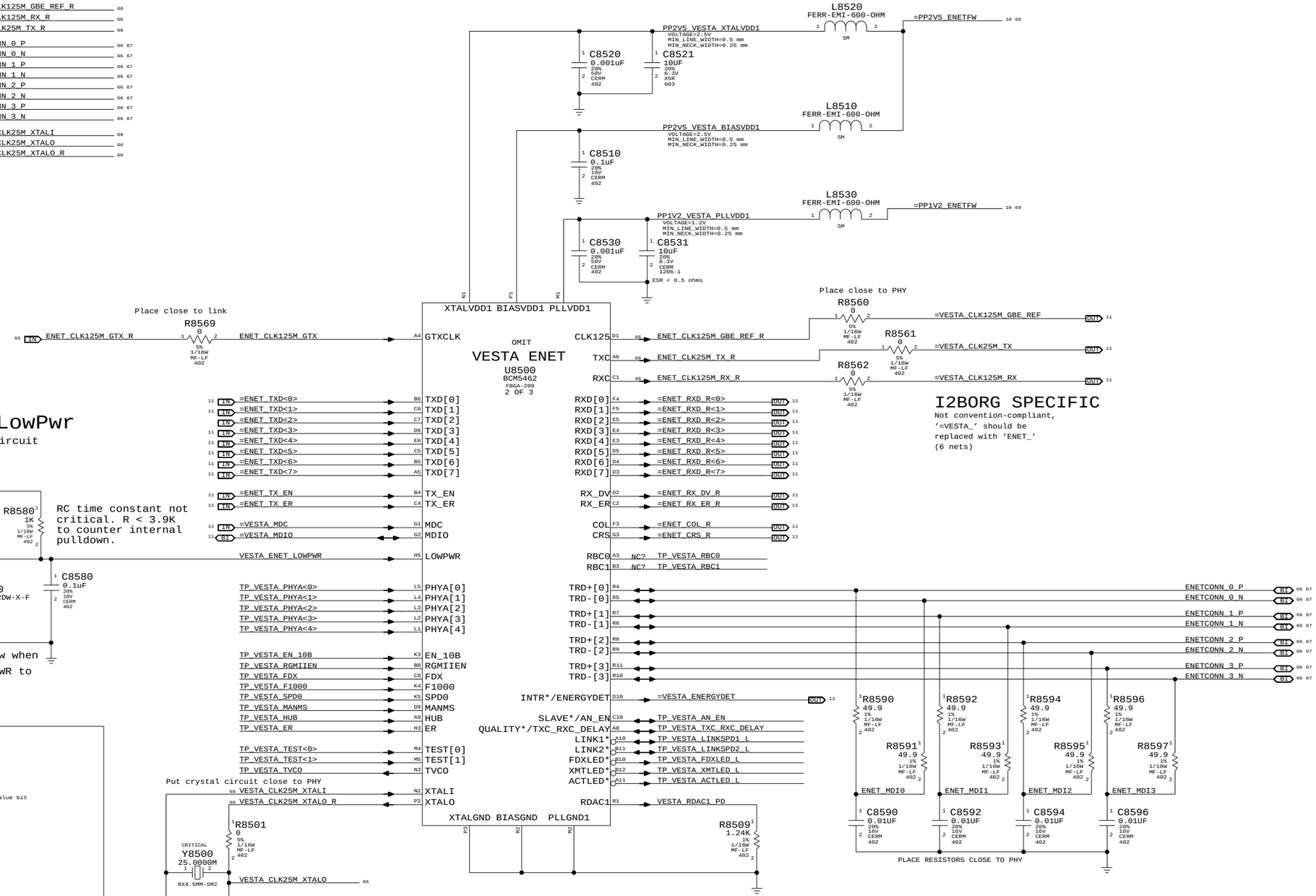
Net Spacing Type: ENET_MDI

~~Line To Line: 0.38 mms~~
~~Length Tolerance: 50 mils~~
~~Primary Max Sep: 5 mils~~
~~Secondary Max Sep: 100 mils~~
~~Secondary Length: 500 mils~~

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Ethernet LowPwr

Disables Vesta Ethernet Circuit



Circuit ensures Vesta LOWPWR signal is low when Vesta RESET* is asserted, and allows LOWPWR to assert when ethernet link is unpowered.

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

Vesta Ethernet PHY

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 85 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
PROVIDED BY ETHERNET PHY	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_P
	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_N
	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_P
	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_N
	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_P
	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_N
	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_P
	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_N

Page Notes

Power aliases required by this page:
- _PP2V5_ENET
- _GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

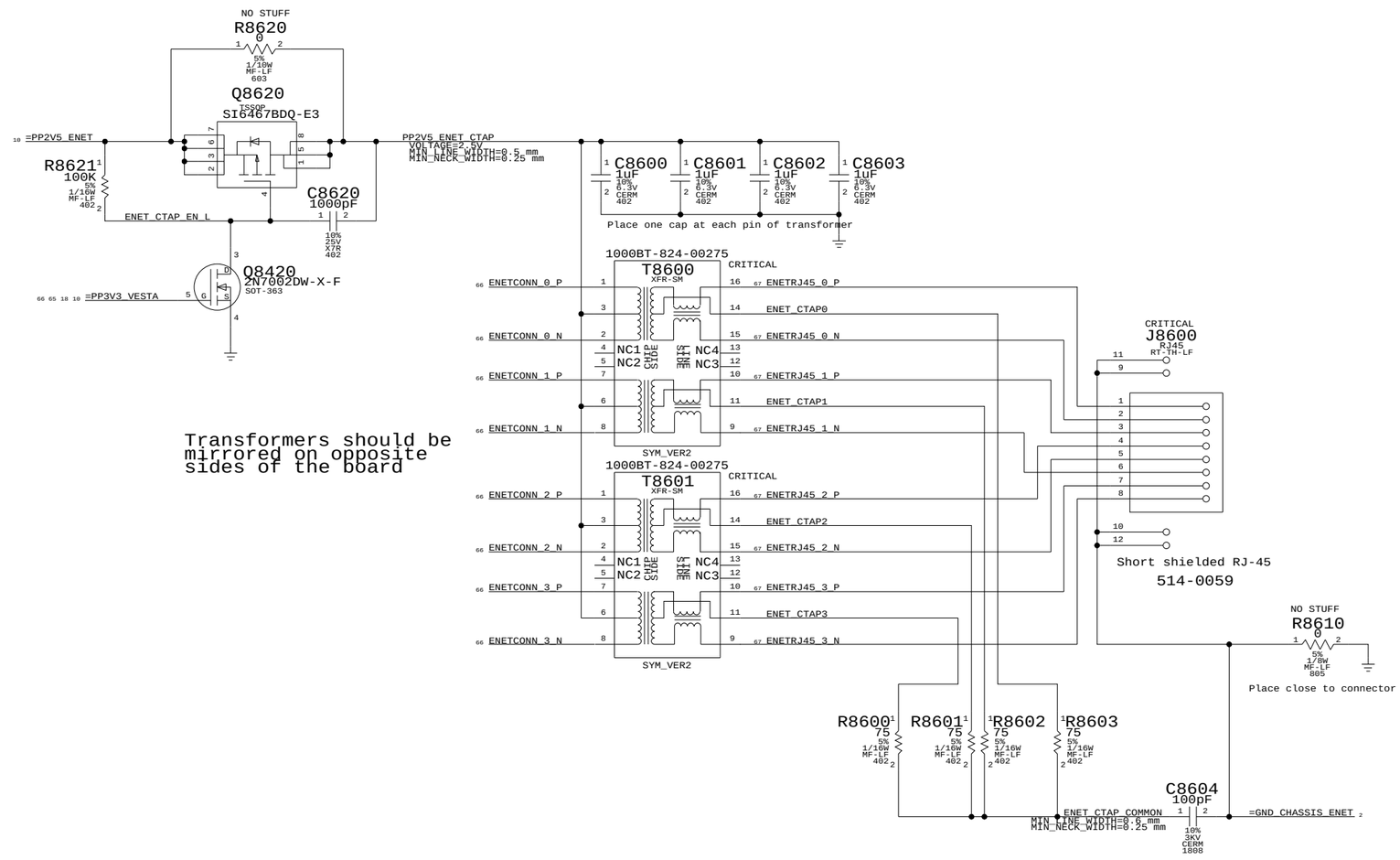
BOM options provided by this page:
(NONE)

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds



Transformers should be mirrored on opposite sides of the board

Ethernet Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 86 OF 115	

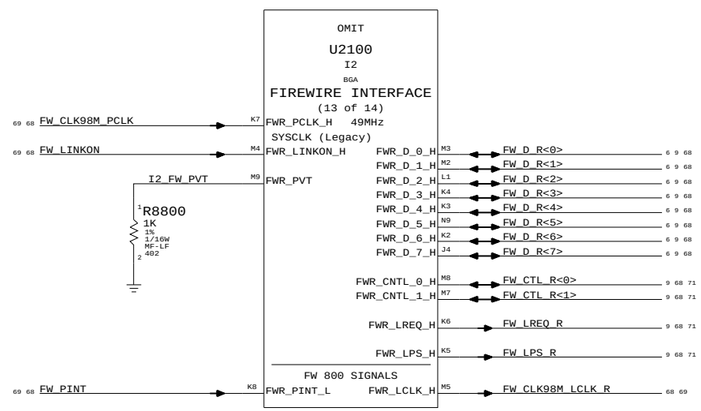
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
FW_D	FW	FW		FW_D_R<7..0>	6 9 68
FW_CTL	FW	FW		FW_CTL_R<1..0>	9 68 71
FW_LREQ	FW	FW		FW_LREQ_R	9 68 71
	FW	FW		FW_LPS_R	9 68 71
	FW	FW		FW_LINKON	68 69
FW_PCLK	CLOCK	CLOCK		FW_CLK98M_PCLK	68 69
FW_LCLK	CLOCK	CLOCK		FW_CLK98M_LCLK_R	68 69
FW_PINT	FW	FW		FW_PINT	68 69

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 FireWire Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 88 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		FW_CLK98M_PCLK_R	69
	CLOCK	CLOCK		FW_CLK98M_LCLK	69
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_P	69 70
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_N	69 70
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_P	69 70
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_N	69 70
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_P	69 70
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_N	69 70
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_P	69 70
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_N	69 70
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_P	69 70
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_N	69 70
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_P	69 70
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_N	69 70
VESTA_CLK24M_XTAL	XTAL	XTAL		VESTA_CLK24M_XTALI	69
	XTAL	XTAL		VESTA_CLK24M_XTALO	69
	XTAL	XTAL		VESTA_CLK24M_XTALO_R	69

Page Notes

Power aliases required by this page:
- =PPFW_PHY_CPS
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

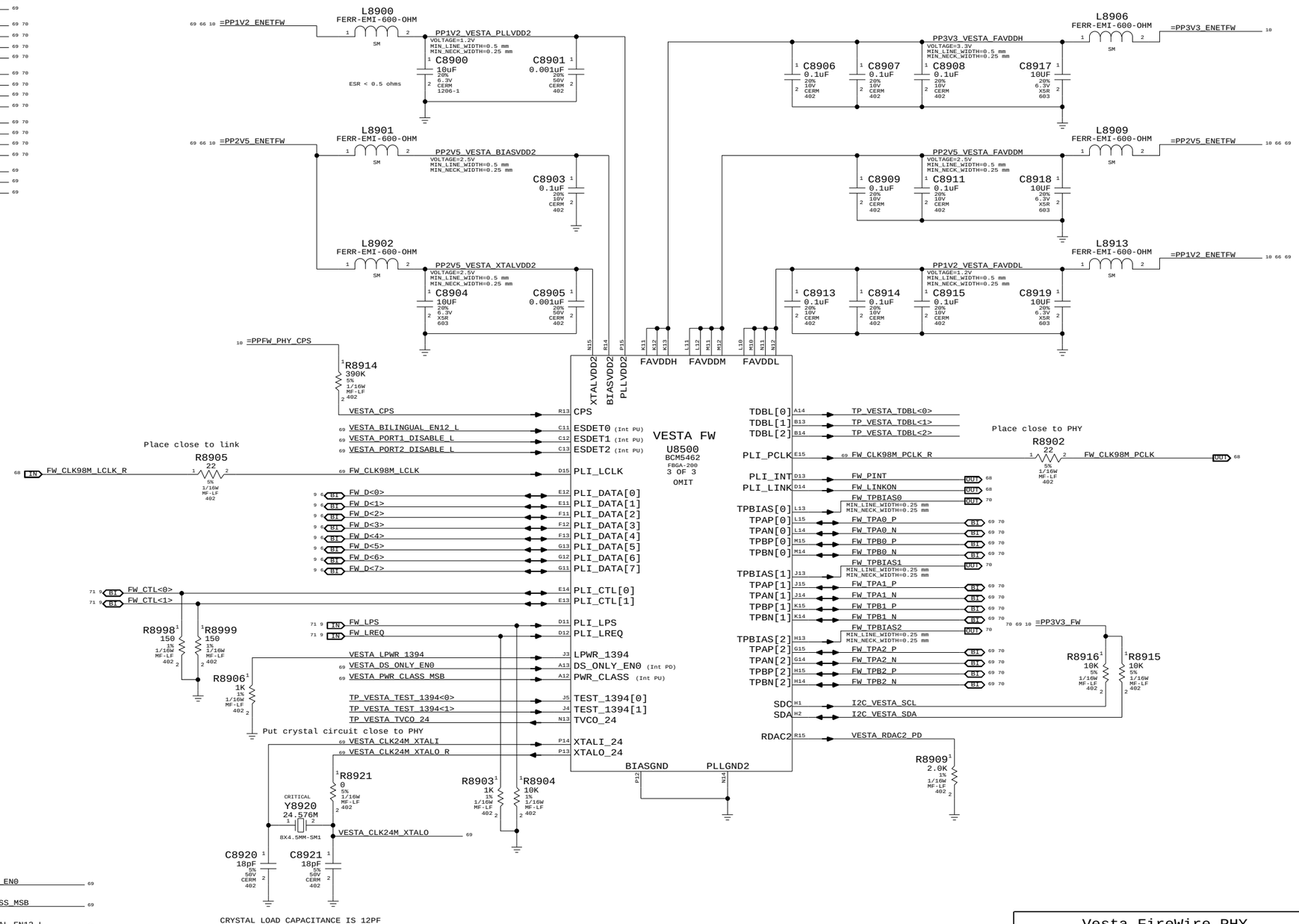
Signal aliases required by this page:
- NONE

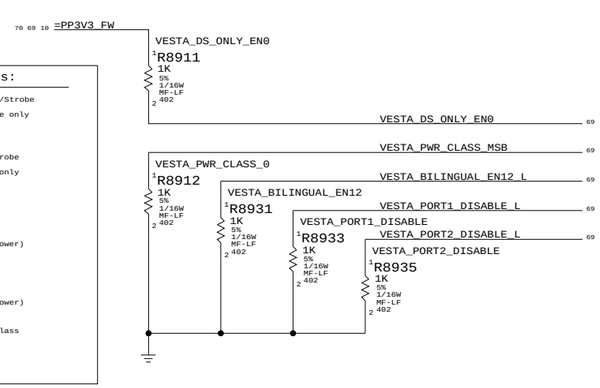
BOM options provided by this page:
- VESTA_BILINGUAL_EN12
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PORT1_DISABLE
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_PORT2_DISABLE
  If stuffed, adds external pull-down to counter internal pull-up in Vesta.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW_TP

Line To Line: 0.38 mms
Length Tolerance: 100 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.





Vesta Config Straps:

DS_ONLY_EN12 - Port 1&2 Data/Strobe
1 - Port 1&2 Data/Strobe mode only
0 - Port 1&2 Bilingual mode
(Internal Pull-up)
DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)
PORT1_ENABLE - Port 1 Enable
1 - Port 1 Enabled
0 - Port 1 Disabled (saves power)
(Internal Pull-up)
PORT2_ENABLE - Port 2 Enable
1 - Port 2 Enabled
0 - Port 2 Disabled (saves power)
(Internal Pull-up)
PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

Vesta FireWire PHY

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 89 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
PROVIDED BY PHY PAGE	FW	FW	FW_PORT1_TPA_FL	FW_PORT1_TPA_P_FL
	FW	FW	FW_PORT1_TPA_FL	FW_PORT1_TPA_N_FL
	FW	FW	FW_PORT1_TPB_FL	FW_PORT1_TPB_P_FL
	FW	FW	FW_PORT1_TPB_FL	FW_PORT1_TPB_N_FL
	FW	FW	FW_PORT2_TPA_FL	FW_PORT2_TPA_P_FL
	FW	FW	FW_PORT2_TPA_FL	FW_PORT2_TPA_N_FL
	FW	FW	FW_PORT2_TPB_FL	FW_PORT2_TPB_P_FL
	FW	FW	FW_PORT2_TPB_FL	FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
- _PPFW_PORT1
- _PPFW_PORT2
- _PPFW_PORT3
- _PP3V3_FW
- _GND_CHASSIS_FW_PORT1
- _GND_CHASSIS_FW_PORT2
- _GND_CHASSIS_FW_PORT3

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

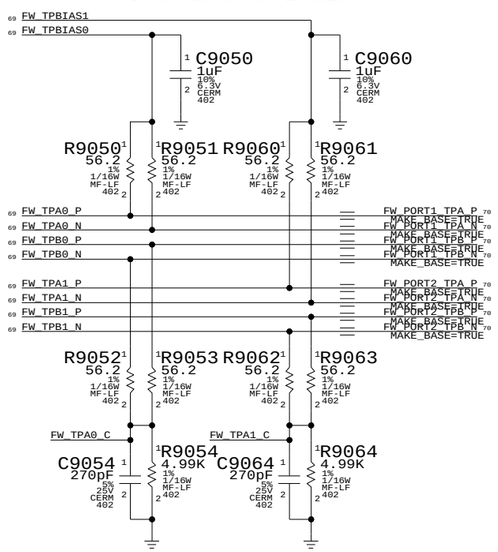
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

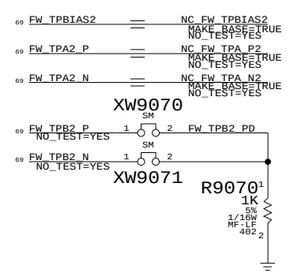
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

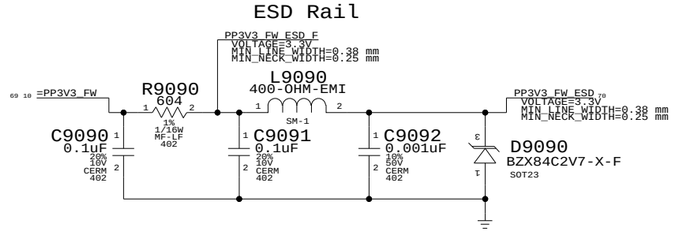
Place close to FireWire PHY



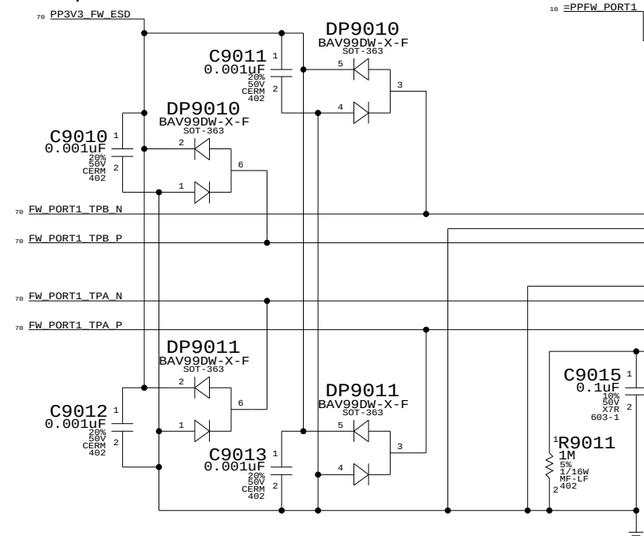
3rd TPA/TPB pair unused



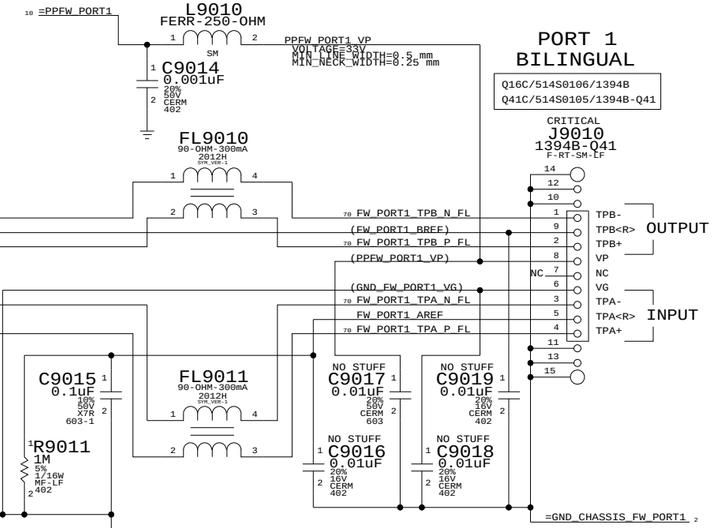
ESD Rail



"Snapback" & "Late VG" Protection



Cable Power



PORT 1 BILINGUAL

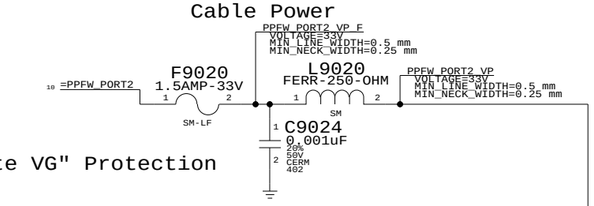
Q16C/514S0106/1394B
Q41C/514S0105/1394B-Q41

AREF needs to be isolated from all local grounds per 1394b spec

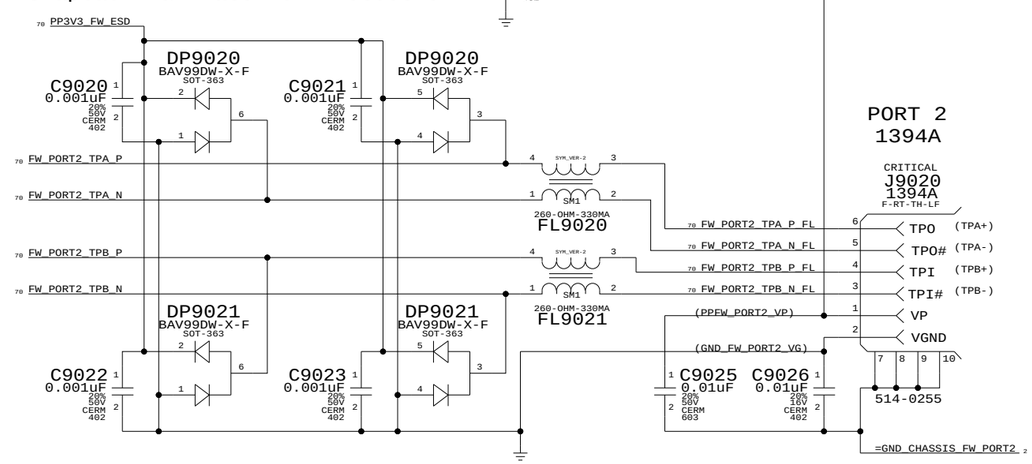
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

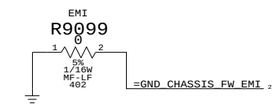
Cable Power



"Snapback" & "Late VG" Protection



PORT 2 1394A



FireWire Ports

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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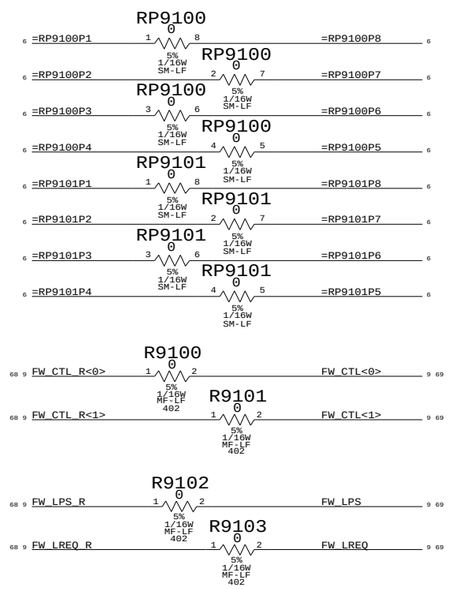
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 90 OF 115	

DRAWING
TITLE=PLASMA
ABBREV=DRAWING
LAST_MODIFIED=Wed Nov 2 16:09:22 2005

Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.).



FireWire Series Term

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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D	051-6839	E
SCALE NONE	SHT 91 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2_P<0>	11 72
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2_N<0>	11 72
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2_P<1>	6 72
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2_N<1>	6 72
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2_P<2>	11 72
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2_N<2>	11 72
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2_P<3>	6 72
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2_N<3>	6 72
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2_P<4>	11 72
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2_N<4>	11 72
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2_P<5>	11 72
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2_N<5>	11 72
USB2_I2_XTAL	XTAL	XTAL		I2_CLK30M_USB2_XOUT_R	72
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XOUT	72
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XIN	72

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

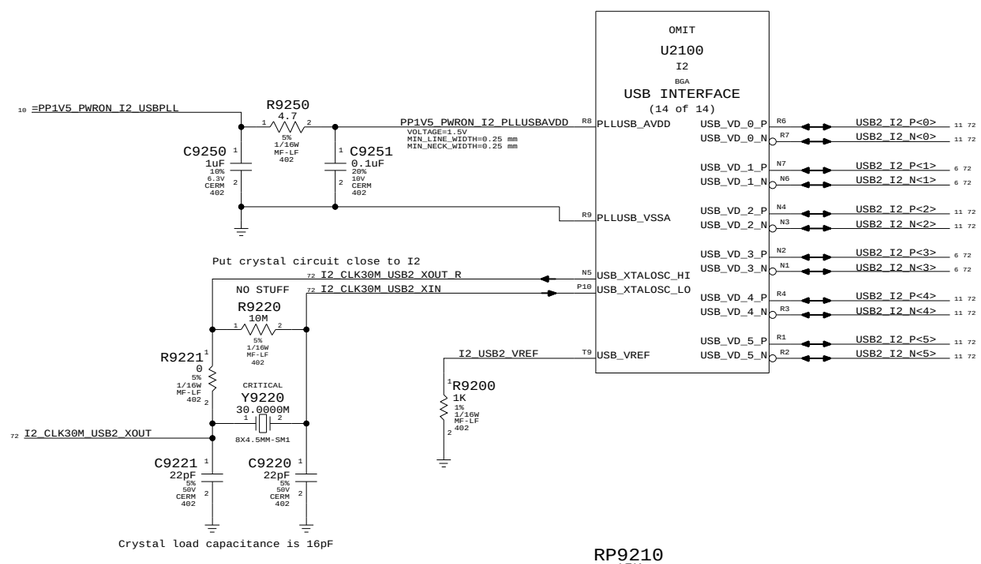
Signal aliases required by this page:
- =RP92xxPy (pinswappable USB pulldowns)

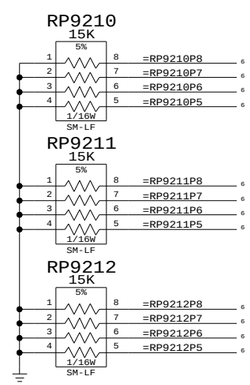
BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

~~Line To Line:~~ 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary ~~Max Sep:~~ 100 mils
~~Secondary~~ Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.





One pair for each port USB2_*<0..5>

I2 USB Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 92 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
ELECTRICAL_CONSTRAINT_SET (PROVIDED BY I2 PAGES)				
E30	USB2	USB2	USB2_NEC_0	USB2_NEC_P<0> 11 73
E31	USB2	USB2	USB2_NEC_0	USB2_NEC_N<0> 11 73
E34	USB2	USB2	USB2_NEC_1	USB2_NEC_P<1> 11 73
E32	USB2	USB2	USB2_NEC_1	USB2_NEC_N<1> 11 73
E33	USB2	USB2	USB2_NEC_2	USB2_NEC_P<2> 11 73
E35	USB2	USB2	USB2_NEC_2	USB2_NEC_N<2> 11 73
E39	USB2	USB2	USB2_NEC_3	USB2_NEC_P<3> 11 73
E37	USB2	USB2	USB2_NEC_3	USB2_NEC_N<3> 11 73
E40 USB2_NEC_XTAL	XTAL	XTAL		NEC_CLK30M_XT1 73
E41	XTAL	XTAL		NEC_CLK30M_XT2 73
E42	XTAL	XTAL		NEC_CLK30M_XT2_R 73

Page Notes

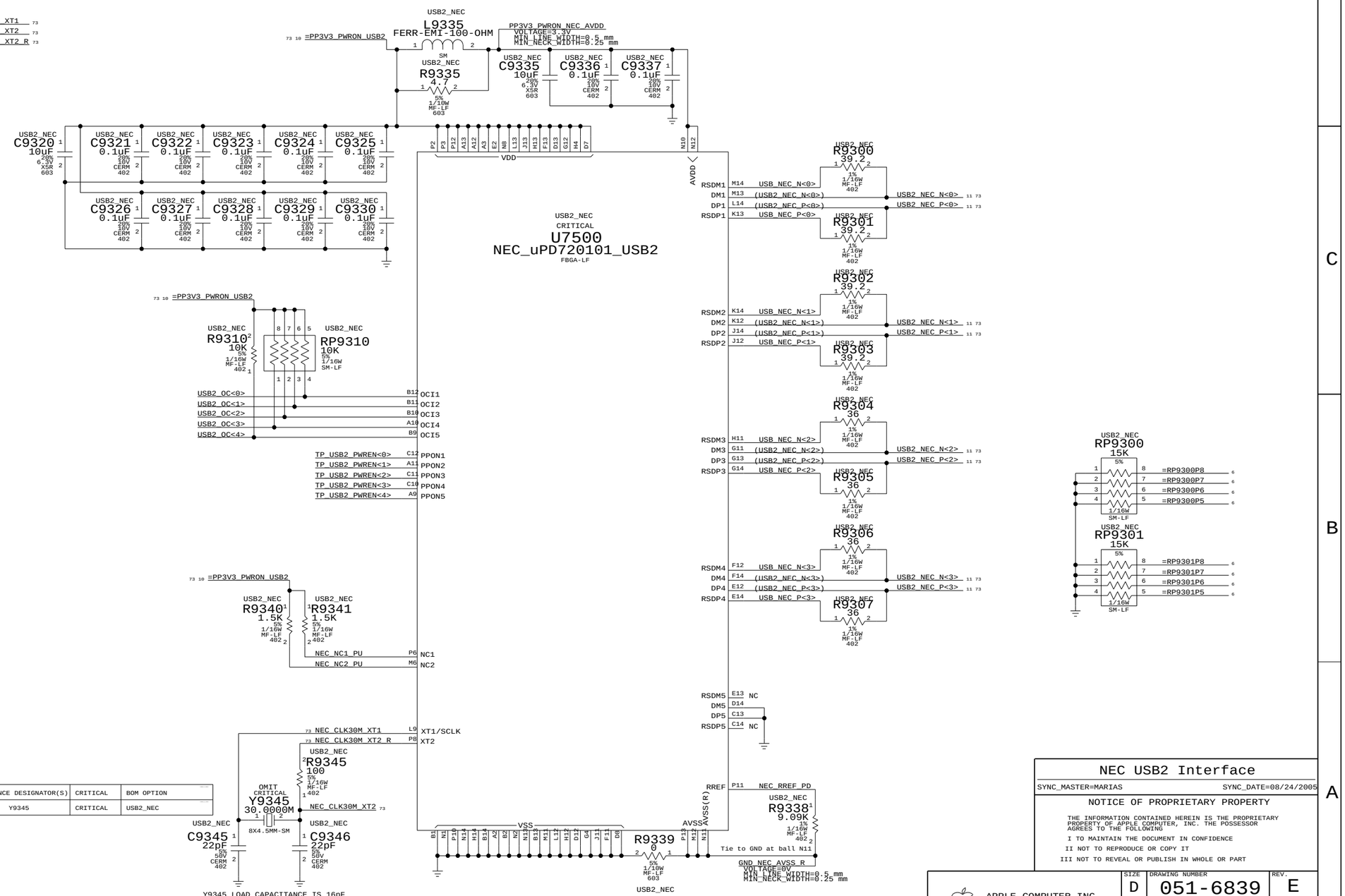
Power aliases required by this page:
- =PP3V3_PWRON_USB2

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,30.0000MHZ,LW PROF,8X4.5MM,SMD	Y9345	CRITICAL	USB2_NEC

NEC USB2 Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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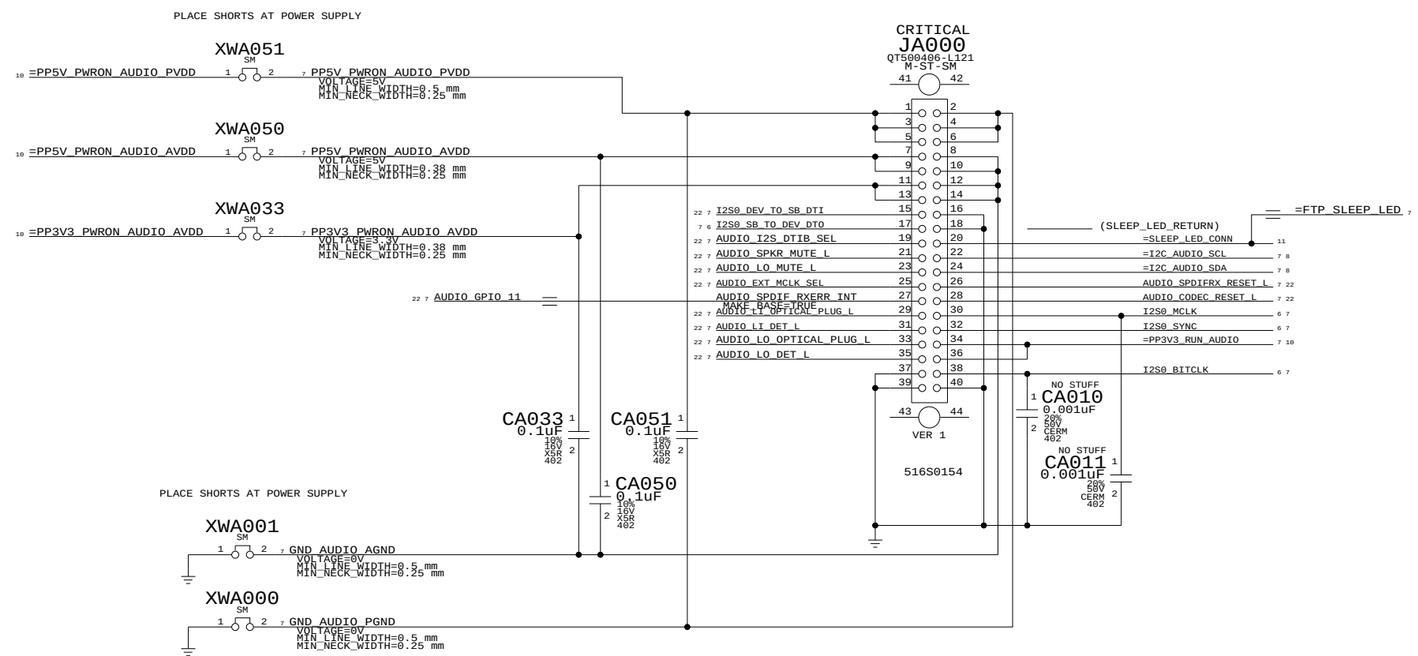
SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE NONE SHT 93 OF 115

AUDIO BOARD CONNECTOR

Place all shorts at output of 3.3V and 5V regulator



Audio Board Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE NONE	SHT 100 OF 115	

AGP

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     AGP          401          *          0.4 MM        =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_SPACING_RULE
     AGP_STB      601          *          0.6 MM         2.5 MM         =100_OHM_DIFF     =100_OHM_DIFF     =100_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     AGP                *        =STANDARD        =60_OHM_SE        =60_OHM_SE        =60_OHM_SE
TABLE_PHYSICAL_RULE
     AGP_STB            *        =STANDARD      =100_OHM_DIFF     =100_OHM_DIFF     =100_OHM_DIFF
```

CLOCK

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     CLOCK        251          *          0.25 MM       =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     CLOCK              *        =STANDARD        =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

ENET (Ethernet Digital)

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     ENET_SELF    =STANDARD    *        =STANDARD       =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_SPACING_RULE
     ENET         201          *          0.2 MM        =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     ENET               *        =STANDARD        =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

```
TABLE_SPACING_ASSIGNMENT
TABLE_SPACING_ASSIGNMENT
     ENET                ENET          *          ENET_SELF
```

FW (FireWire Digital)

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     FW_SELF      =STANDARD    *        =STANDARD       =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_SPACING_RULE
     FW           201          *          0.2 MM        =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     FW                 *        =STANDARD        =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

```
TABLE_SPACING_ASSIGNMENT
TABLE_SPACING_ASSIGNMENT
     FW                  FW            *          FW_SELF
```

I2C

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     I2C          201          *          0.2 MM        =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     I2C                *        =STANDARD        =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

MaxBus

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     MAXBUS       151          *          0.15 MM       =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     MAXBUS             *        =STANDARD        =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

PCI

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     PCI          =STANDARD    *        =STANDARD       =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     PCI                *        =STANDARD        =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

RAM

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     RAM          201          *          0.2 MM        =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_SPACING_RULE
     RAM_DIFF     251          *          0.25 MM        2.5 MM         =100_OHM_DIFF     =100_OHM_DIFF     =100_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     RAM                *        =50_OHM_SE       =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
TABLE_PHYSICAL_RULE
     RAM_DIFF           *      =100_OHM_DIFF    =100_OHM_DIFF     =100_OHM_DIFF     =100_OHM_DIFF
```

UATA

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     UATA         151          *          0.15 MM       =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     UATA               *        =50_OHM_SE       =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

USB2

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     USB2         501          *          0.50 MM        3.81 MM         =90_OHM_DIFF      =90_OHM_DIFF      =90_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     USB2               *        =90_OHM_DIFF     =90_OHM_DIFF      =90_OHM_DIFF      =90_OHM_DIFF
```

AUDIO

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     AUDIO        251          *          0.25 MM       =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     AUDIO              *        =50_OHM_SE       =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

I2S

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     I2S          251          *          0.25 MM       =STANDARD         =STANDARD         =STANDARD         =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     I2S                *        =50_OHM_SE       =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

ENETCONN

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     ENETCONN     501          *          0.50 MM        3.81 MM         =100_OHM_DIFF     =100_OHM_DIFF     =100_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     ENETCONN           *      =100_OHM_DIFF    =100_OHM_DIFF     =100_OHM_DIFF     =100_OHM_DIFF
```

FW_TP

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     FW_TP        501          *          0.50 MM        3.81 MM         =110_OHM_DIFF     =110_OHM_DIFF     =110_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     FW_TP              *      =110_OHM_DIFF    =110_OHM_DIFF     =110_OHM_DIFF     =110_OHM_DIFF
```

I2_FBCLK / XTAL

```
TABLE_SPACING_ASSIGNMENT
TABLE_SPACING_ASSIGNMENT
     I2_FBCLK           *                *            CLOCK
TABLE_SPACING_ASSIGNMENT
     XTAL               *                *            CLOCK
TABLE_PHYSICAL_ASSIGNMENT
TABLE_PHYSICAL_ASSIGNMENT
     I2_FBCLK           *            CLOCK
TABLE_PHYSICAL_ASSIGNMENT
     XTAL               *            CLOCK
```

Spacing & Physical Constraints

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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D	051-6839	E
SCALE NONE	SHT 110 OF 115	

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     DVO          151        *        0.15 MM      =STANDARD       =STANDARD       =STANDARD       =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     DVO                *        =STANDARD      =50_OHM_SE        =50_OHM_SE        =50_OHM_SE
```

DVO

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     TV           151        *      =75_OHM_SE     =75_OHM_SE      =75_OHM_SE      =75_OHM_SE      =75_OHM_SE
TABLE_SPACING_RULE
     TV_CONN      151        *          =TV            =TV             =TV             =TV             =TV
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     TV                *      =75_OHM_SE     =75_OHM_SE      =75_OHM_SE      =75_OHM_SE
TABLE_PHYSICAL_RULE
     TV_CONN           *          =TV            =TV             =TV             =TV
```

S-VIDEO

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     VGA          151        *      =75_OHM_SE     =75_OHM_SE      =75_OHM_SE      =75_OHM_SE      =75_OHM_SE
TABLE_SPACING_RULE
     VGA_CONN     151        *          =VGA           =VGA            =VGA            =VGA            =VGA
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     VGA               *      =75_OHM_SE     =75_OHM_SE      =75_OHM_SE      =75_OHM_SE
TABLE_PHYSICAL_RULE
     VGA_CONN          *          =VGA           =VGA            =VGA            =VGA
```

VGA

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     LVDS         151        *                 =100_OHM_DIFF   =100_OHM_DIFF   =100_OHM_DIFF   =100_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     LVDS              *    =100_OHM_DIFF  =100_OHM_DIFF    =100_OHM_DIFF    =100_OHM_DIFF
```

LVDS

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     TMDS         251        *        0.25 MM      =100_OHM_DIFF   =100_OHM_DIFF   =100_OHM_DIFF   =100_OHM_DIFF
TABLE_SPACING_RULE
     TMDS_CONN    =TMDS      *          =TMDS          =TMDS           =TMDS           =TMDS           =TMDS
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     TMDS              *    =100_OHM_DIFF  =100_OHM_DIFF    =100_OHM_DIFF    =100_OHM_DIFF
TABLE_PHYSICAL_RULE
     TMDS_CONN         *          =TMDS          =TMDS           =TMDS           =TMDS
```

TMDS

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     THERM        251        *        0.25 MM      =100_OHM_DIFF   =100_OHM_DIFF   =100_OHM_DIFF   =100_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     THERM             *        Y            0.25 MM         =100_OHM_DIFF    =100_OHM_DIFF
```

THERM

Spacing & Physical Constraints 2

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E

SCALE NONE SHT 111 OF 115

*** Signal Cross-Reference for the entire design ***

1V5RUN_EN 16A6<> 26C6<
1V8RUN_EN_L 16A4<> 26B4<>
1V8_1V5PWRON_EN_L 26D4<
1V20_REF 12C7< 14C8<
1V65_REF 13A5<
1_5V_BOOST 16C6<>
1_5V_BST 16C5<>
1_5V_DH 16C6<>
1_5V_DL 16B6<>
1_5V_FB 16B7<
1_5V_ILIM 16C5<>
1_5V_LX 16B5<>
1_8V_BOOST 16C4<>
1_8V_BST 16C4<>
1_8V_DH 16C3<>
1_8V_DL 16B3<>
1_8V_FB 16B4<
1_8V_ILIM 16C5<>
1_8V_LX 16B3<>
1_8V_PVDD_STD 51C1<
2V5PWRON_EN_L 26D4<
2V5RUN_EN_L 17A5<> 26C6<
3V3RUN_EN_L 15B3<> 26C5<
3V_BG 15C4<>
3V_BOOST 15C4<>
3V_BOOST_ESR 15D3<>
3V_ITH 15C4<>
3V_ITH_RC 15C3<
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=GND_CHASSIS_FW_HOLE 2D1<> 2D4>
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=I2C_DS1775_SDA 7C5> 8B1> 30C6<>
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=I2C_I2_SB_SDA 8D3< 22B2<
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=I2_AGP_VREF 11C7> 43B5<
=I2_MAXBUS_FBCLK_IN 21D1> 32A6<
=I2_PCI_FBCLK_IN 21B5> 59A5<
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=I2_STOPXTAL_L 11B3> 22A5<
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=PCI_AIRPORT_IDSEL 11C1> 60C7<
=PCI_AIRPORT_INT_L 11C1> 60B3<>
=PCI_AIRPORT_REQ_L 11D1> 60C5<>
=PCI_AIRPORT_RESET_L 11C1> 60C3<>
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=PCI_CBUS_IDSEL 11C1> 61B8<
=PCI_CBUS_INT_L 11C1> 61A7<>
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=PCI_CLK33M_USB2 11C1> 62B5< 62D6>
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=PP1V2_VESTA_REG 10D6< 18C1<
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=PP1V5R1V8_MAXBUS 10A1> 21C8< 32D1< 33A5< 33B8< 33C8< 34B5< 34B7< 34C4< 34C4< 34D4<
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=PP1V5R1V8_RUN_I2_MAXBUS 10A1> 32B5<
=PP1V5R3V3_DVO_VREF 47C1> 54A2<
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=PP1V5_GPU_DVO 10A6> 47C2<
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=PP1V5_GPU_VDD15 10A6> 46B5<>
=PP1V5_I2_AGP 10A4> 43C7<
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=PP1V5_PWRON_I2_PLL 10D1> 19C5<
=PP1V5_PWRON_I2_USBPLL 10D1> 72C7<
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=PP1V5_RUN_RUNFET 10A3> 16A6<>
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=PP2V5_RUN_RUNFET 10B3< 17B4<>
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=PP2V8_GPU_LVDS_IO 10B6> 47A1<
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=PP3V3_ALL_AC_DETECT 10C6> 12C7<>
=PP3V3_ALL_BATT0_DET 10B6> 12B7<
=PP3V3_ALL_BATT_CHGR 10C6> 13A6<> 13A8< 13C8<
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=PP3V3_ALL_HALL_EFFECT 10C6> 30D6<
=PP3V3_ALL_LTC1625_SW 10C6> 14C7<>
=PP3V3_ALL_PBUS_ILIM 10C6> 13C3< 13D4<
=PP3V3_ALL_PMU 10C6> 24A7< 24D7< 25B6< 25C8< 25D5<
=PP3V3_ALL_PWRSEQ 10B6> 26B7<> 26D5<
=PP3V3_ALL_VREG 10C8< 14A2<
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=PP3V3_BATT_IMON 10B6> 12A5<
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=PP3V3_DDC_LCD 7B7> 10B1> 56C7<>
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=PP3V3_FW 10D4> 69A8< 69B2< 70A8<
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=PP3V3_PCI_AIRPORT 10B1> 60C3<>
=PP3V3_PCI_ROM 10B5< 58B6< 58C5<>

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=PP3V3_PWRON_CPUVCORE_OFFSET 10B3> 36B7<
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=PP3V3_PWRON_I2_AGPPCI 10B5< 19A5<
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=PP3V3_PWRON_I2_MAXBUS 10B4> 19B5<
=PP3V3_PWRON_I2_MISC 10B5< 22B6< 22C7<
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=PP3V3_PWRON_LCD 10B4> 56C8<>
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=PP3V3_PWRON_LTC3412 10B4> 17D6<
=PP3V3_PWRON_MMM 10B4> 29C6<
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=PP3V3_PWRON_RT_ALS 10B5< 28D5<
=PP3V3_PWRON_RUNFET 10B4> 15B2<>
=PP3V3_PWRON_TPS2211 10B4> 61D4<
=PP3V3_PWRON_USB2 10A4> 73B6< 73C6< 73D5<
=PP3V3_PWRON_VDDSPD 10B5< 40A6<> 41A4<> 41A6<>
=PP3V3_PWRON_VGASYNC 10B4> 57C2< 57C2<
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=PP3V3_RUN_FANTACH 10B1> 27D2<
=PP3V3_RUN_FWPORTPWRSW 10B1> 18C8<
=PP3V3_RUN_HDD 10B1> 64B8< 64C7<
=PP3V3_RUN_KEYBRD_LED 10B1> 28B6<
=PP3V3_RUN_PCI1510_R 10B1> 61D7<
=PP3V3_RUN_PWRSEQ 10B3< 26B7<
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=PP3V3_RUN_SI 10B1> 54C2< 54C3< 54C5< 55C3< 55D3< 55D3<
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=PP3V3_VESTA_2V5REG 10D4> 18D3<>
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=PP5V_PWRON_CPUVCORE_VDD 10C4> 36C6<>
=PP5V_PWRON_GPUVCORE_PWRPLAY 10C3> 45B5<
=PP5V_PWRON_INVERTER 10B4> 56C4<>
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=PP5V_PWRON_RUNFET 10C4> 15B5<>
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=PP5V_PWRON_TRACKPAD 10B4> 15B8<>
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=PP5V_RUN_FANPWM 10C1> 27D2<
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=PP12V8_PBUSB_HOLDUP_CAPS 10D6> 31D3<
=PP12V8_PBUS_PMU_SUPPLY 10D6> 14A7<>
=PP14VR24V_ALL_PBUS_A 10D8< 13D5<
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=PP24V_ADAPTER_PMU_SUPPLY 10C6> 14A7<
=PP24V_ADAPTER_RAW 10C6> 12D8<>
=PP24V_PBUSA_HOLDUP_CAPS 10D6> 31D5<
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SIZE D | DRAWING NUMBER 051-6839 | REV. E
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*** Part Cross-Reference for the entire design ***

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U1200	COMPARATOR_LMC7211	12
U1220	COMPARATOR_LMC7211	12
U1250	INA138	12
U1300	MAX1772	13
U1350	COMPARATOR_LMC7211	13
U1370	AMP_MAX4172	13
U1380	OPAMP_LMC7111	13
U1400	LTC1625	14
U1420	COMPARATOR_LMC7211	14
U1450	VREG_LP2951	14
U1460	VREG_LP2951	14
U1500	LTC3707	15
U1600	MAX1715	16
U1700	LTC3412	17
U1970	VREG_LM2594	18
U1980	VREG_MM1572FN	18
U1990	LTC3411	18
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U2500	CLK_DR_CDCVF2505	23
U2700	M38280F8	25
U3000	ADT7467	27
U3100	OPAMP_MAX4236EUTT	28
U3130	MM3120	28
U3220	KXM52	29
U3600	A8	33 34 35
U3900	MAX1717	36
U3990	PI3B3257	36
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U5800	LTC1778	45
U6200	SDRAM_DDR_K4D553235F	49
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U6953	NC7S32	56
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U7051	741G32	57
U7070	COMPARATOR_LMC7211	57
U7100	FEPR_1MX8	58
U7400	PCI1510GGU	61
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Y9220	CRYSTAL	72
Y9345	CRYSTAL	73

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